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Advanced Indium Antimonide Monolithic Charge Coupled Infrared Imaging Arrays

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Langley Research Center
Hampton, Virginia 23665

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ADVANCED INDIUM ANTIMONIDE (InSb) MONOLITHIC CHARGE COUPLED INFRARED IMAGING ARRAYS

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FINAL REPORT

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Hampton, Virginia 23665

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FOREWORD

This Final Report was prepared by Santa Barbara Research Center, Goleta, California, under Contract No. NAS1-16383. The technical effort was performed during the period of 10 September 1980 to 10 June 1981. The work was sponsored by the Langley Research Center, National Aeronautics and Space Administration. The Technical Representative for NASA was William E. Miller. The Program Manager was Richard D. Thom; the Project Engineer was Thomas L. Koch.

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SYMBOLS

ρ = oxide resistivity, ohm-cm

ψ = relative amplitude change in ellipsometer

ψ_s = surface potential, volts

Δ = relative phase change in ellipsometer

η = detector quantum efficiency

n_f = index of refraction

k = absorption coefficient

A_G = area of gate, cm^2

C_{ox} = oxide capacitance per unit area, F/cm^2

CTE = charge transfer efficiency (efficiency per transfer)

K_{ox} = oxide dielectric constant

N_D = substrate net impurity concentration, cm^{-3}

N_{FC} = number of oxide charges per unit area = Q_{FC}/q, cm^{-2}

N_{SS} = surface state density, $\#/cm^2$-eV

t_{ox} = oxide thickness, cm (1Å = 10^{-8} cm)

T_S = storage time, seconds

V_{FB} = flatband voltage, volts

V_G = applied gate voltage, volts

Section 1
INTRODUCTION

Future infrared sensors will benefit in reduced weight, volume, and power requirements of the detector array and associated electronics through the use of monolithic integrated detector charge-coupled infrared imaging devices (CCIRIDs). CCIRIDs may be configured in linear or area array configurations and can be used for either staring or scanning applications. Scanning configurations designed to operate in time delay and integration (TDI) modes will allow a square root in the number of detectors improvement in the detected signal. Such devices should be capable of operating at high speeds with excellent charge transfer efficiencies (CTE) and have on-chip amplifying MISFETs with high transconductance values.

The long-range objective of this work is to develop a new concept in infrared imaging sensors utilizing charge transfer techniques. These devices are intended for use in the infrared spectral range from 1 to 5.4 μm, and are to be used for remote sensing of the earth's environment (from spacecraft and/or aircraft) and other objects in the solar system, e.g., astronomy and planetary imaging applications, as well as other IR imaging applications.

Indium antimonide (InSb) has been one material of interest for developing CCIRIDs to meet the 1- to 5.4-μm spectral requirement. Ingots of InSb can be grown with relatively high purity, low dislocation density, and in sufficient size to permit wafer diameters in the 2.5- to 4.0-cm range, suitable for convenient handling and photolithography. It is more tolerant to exposure to elevated temperatures during processing than other narrow-bandgap materials and permits diffusion or annealing cycles up to 400°C before surface decomposition begins to occur.

BACKGROUND

The feasibility of InSb monolithic CCIRIDs has been the intention of development efforts conducted under NASA funded contracts since 1973. During the course of these contracts, four generations of CCIRID designs have been generated and several major milestones have been achieved in CCIRID operational characteristics. An important milestone was achieved under Contract NAS1-13163 with the first successful fabrication and demonstration of charge transfer in an InSb CCD.[1] The relatively low CTE of these first devices (0.90) was due to

limitations in achievable gate dimensions at that time. This was improved by dimensional reductions in a second chip design which allowed the CTE to increase to 0.975.[2]

During Contract NAS1-14922, the first monolithic InSb CCD array, integrating a linear array of 20 MOS detector elements with an InSb CCD multiplexer, was achieved.[3] Photomicrographs of 1) an initial and completed SBRC 8585 InSb wafer, 2) an overall SBRC 8585 chip, and 3) a 20-element monolithic InSb CCIRID array are shown in Figure 1. These devices are typified by CTE values ranging from ~0.990 to ~0.997. A typical output for one of these devices is shown in Figure 2.

During Contract NAS1-15551 the performance characteristics of the 20-element InSb CCD arrays were further evaluated and improved operational characteristics were obtained.[4] Detectivity measurements for one array were made using a clamped sample-and-hold amplifier. Data for this array, clocked in the multiplexing mode, are shown in Figure 3. Under low background conditions, single-element peak detectivity values exceeding 8×10^{11} cm-Hz$^{1/2}$-watt^{-1} and an array detectivity average of 6.4×10^{11} cm-Hz$^{1/2}$-watt^{-1} were measured. Other radiometric characteristics of the InSb arrays, including quantum efficiency, linearity and dynamic range, were also evaluated and reported.[5,6]

Operation of the 20-element InSb CCD arrays with the transfer gate timing changed to obtain TDI of the detector signals has also been evaluated. At a clock frequency of f_c = 500 Hz and T = 59K, a measured TDI peak detectivity of 8×10^{12} cm-Hz$^{1/2}$-watt^{-1} was achieved.

Evaluation of the detector quantum efficiency (η) was performed, and a value of $\eta \simeq 0.5$ measured. This verifies the quantum efficiency advantage of intrinsic detector materials as compared to monolithic Si:X arrays, for which η is approximately a factor of two lower. This value was limited by the use of thin (~75Å) titanium photogates in these devices. A replacement structure using an indium-tin-oxide conductive layer has been developed for which computer analysis predicts the photogate structure transmission should increase from 50 to greater than 70% over the 2.5- to 5.4-μm range. With this improvement incorporated, a proportional improvement in quantum efficiency should be attained.

Two 20-element InSb devices were delivered to NASA for evaluation in 1978 on Contract NAS1-14922 and two additional arrays with similar characteristics

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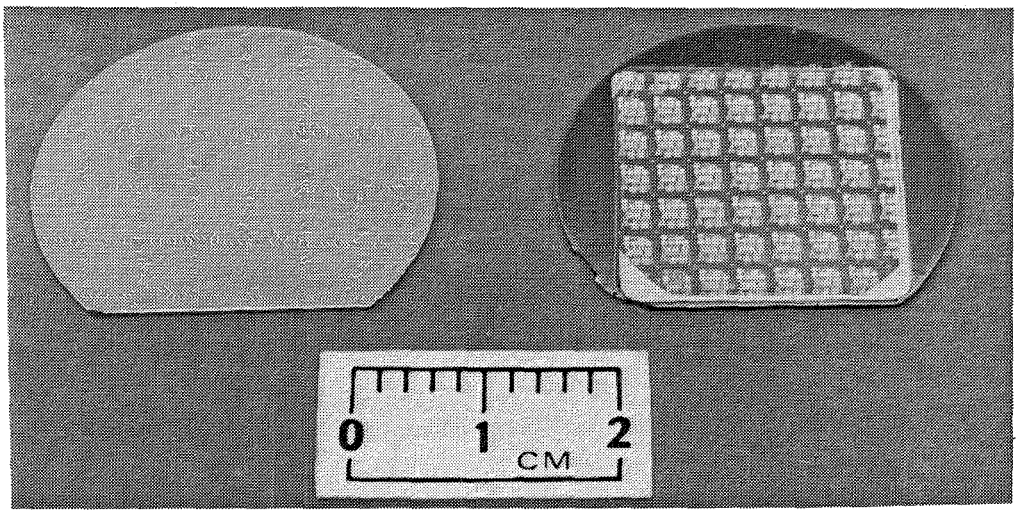

(a) InSb CCIRID Wafers

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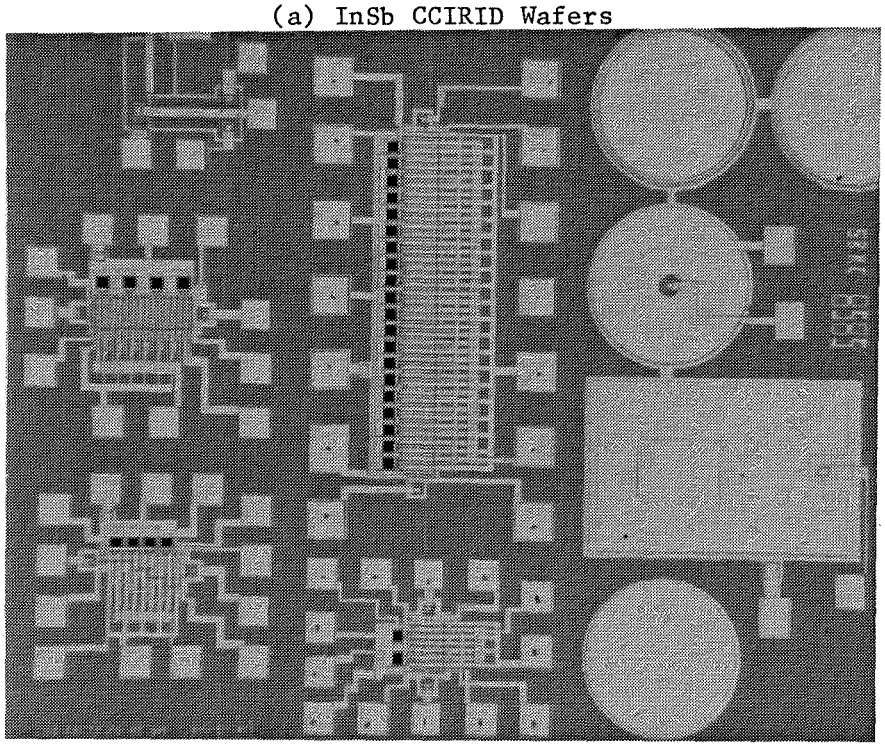

(b) SBRC 8585 InSb CCIRID Chip

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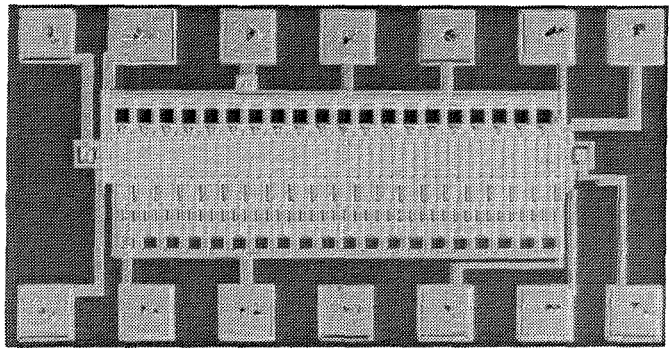
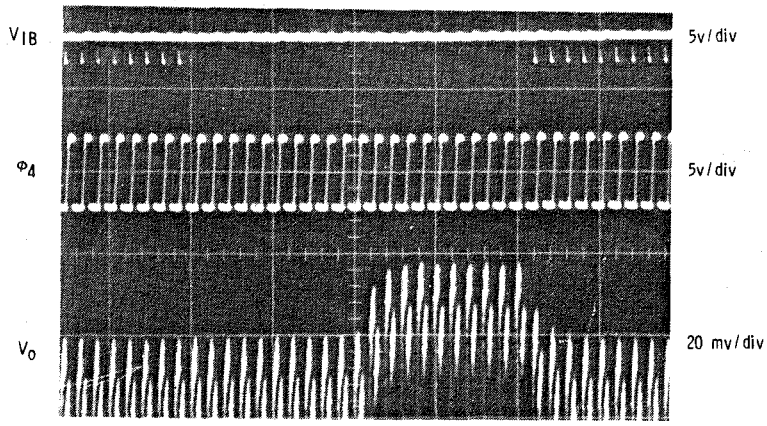


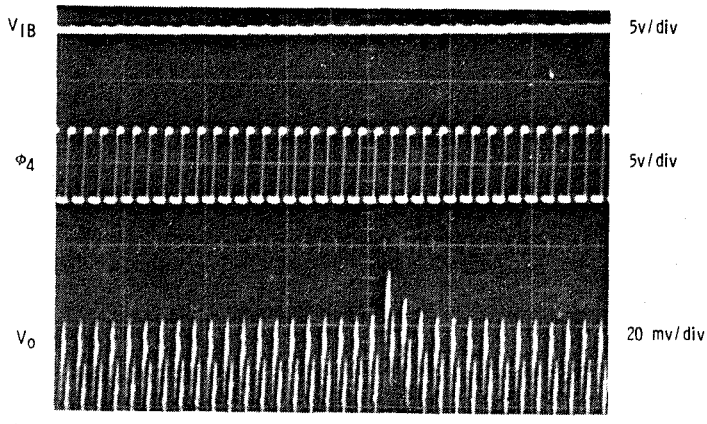
(c) 20-Element InSb CCIRID

Figure 1. Monolithic InSb CCIRID



500 μsec/div

(a) TEN INPUT PULSES

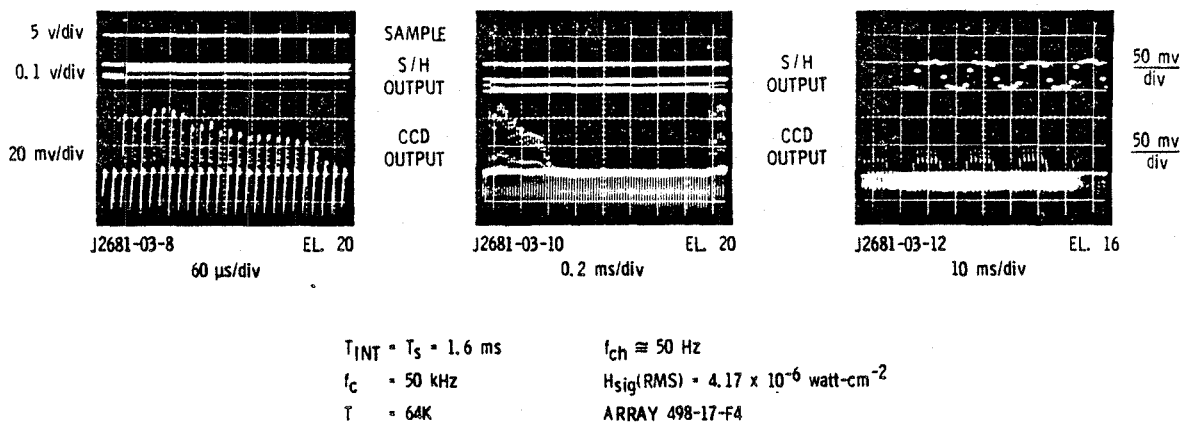


500 μsec/div

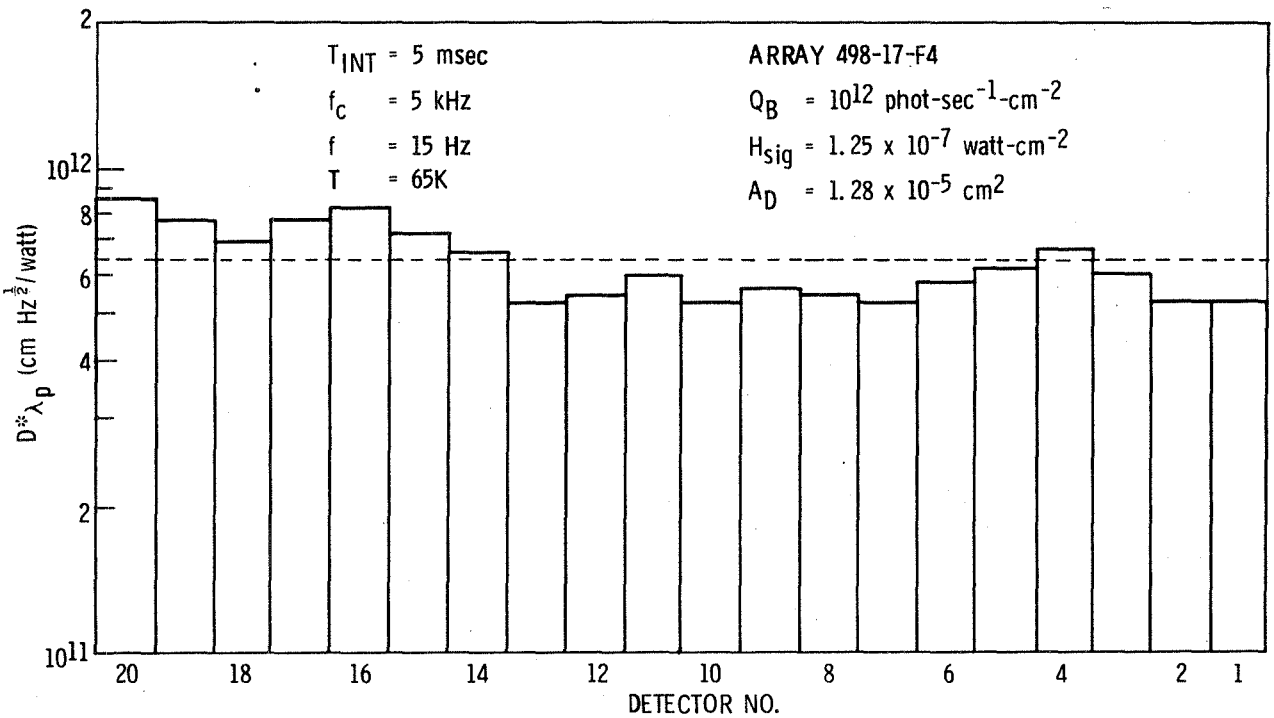
(b) SINGLE INPUT PULSE

f_c	= 10 kHz	V_{OG}	= -4.4 volts
T	= 63 K	V_{REF}	= -1.0 volt
V_{ID}	= 0	ΦRST	= -1.5 to -9.5 volts
V_{SC}	= -7.8 volts	V_{DD}	= -10 volts
Φ_1	= -0.8 to -2.6 volts	V_{SS}	= +5 volts
Φ_2	= -3 to -7 volts	V_{CS}	= -1.2 volt
Φ_3	= -0.6 to -2.0 volts	Φ_T	= 0
Φ_4	= -3 to -7 volts	Φ_P	= 0

Figure 2. Output of 20-Element InSb CCIRID No. 498-17-A3 (Retest, Four Months after Packaging); CTE = 0.9955 ± 0.0005



(a) Sample-and-Hold of 20-Element InSb CCD Array Output



(b) Measured Detectivity of 20-Element InSb CCD Array in Multiplexing Mode

Figure 3. Output Signal and Measured Detectivity Data for 20-Element InSb CCIRID

were delivered on Contract NAS1-15551. Further evaluation of the deep space astronomy applications for these devices is being conducted by operating one of the originally delivered 20-element imagers in the Space Infrared Telescope Facility (SIRTF) under a joint Langley Research Center and Ames Research Center program. Finally, a prototype imaging facility is being assembled at Langley Research Center to demonstrate the utility and capability of these devices to potential users.

Under NASA Contract NAS1-15551 a next-generation mask set (SBRC 8587) was designed and procured which extends the monolithic technology from linear to area arrays. The SBRC 8587 chip (Figure 4) incorporates two principal devices: a 20×16 TDI imaging array, and a 100-element linear array, plus several other test devices. In addition, the chip includes optional interconnect patterns for incorporating on-chip, as well as off-chip, output MISFET amplifiers. Incorporating the output interconnection scheme allows the design to be used for other semiconductor materials, such as HgCdTe, in addition to InSb. Initial evaluation of the SBRC 8587 design was carried out and reported on Contract NAS1-15954.* One each of the 20×16 TDI area array and 100-element linear array chips were packaged and delivered to NASA Langley Research Center for evaluation upon completion of that contract.

PROGRAM OBJECTIVES

Although the reported operational characteristics of the delivered InSb CCIRIDs are considered quite good, they are insufficient to meet the required CTE values (>0.999) projected for future system needs.[7] To achieve useful performance levels, they are critically dependent on the MIS interface characteristics and must have very low N_{SS} which is stable during subsequent processing and device operation. IR&D funded research efforts in InSb surface passivation have resulted in the following basic approach to meet these requirements:

1. utilize accurately-oriented (111)B wafers and prepare the surface so as to preserve or attain the highest degree of atomic order;
2. grow a very thin natural oxide to tie up the surface dangling bonds with minimum disruption of In-Sb bonds beneath the interface; and

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* T.L.Koch, R.D.Thom, and P.E.Herning, "Development of Monolithic Infrared Imaging Array Technology", Contract NAS1-15954, unpublished paper.

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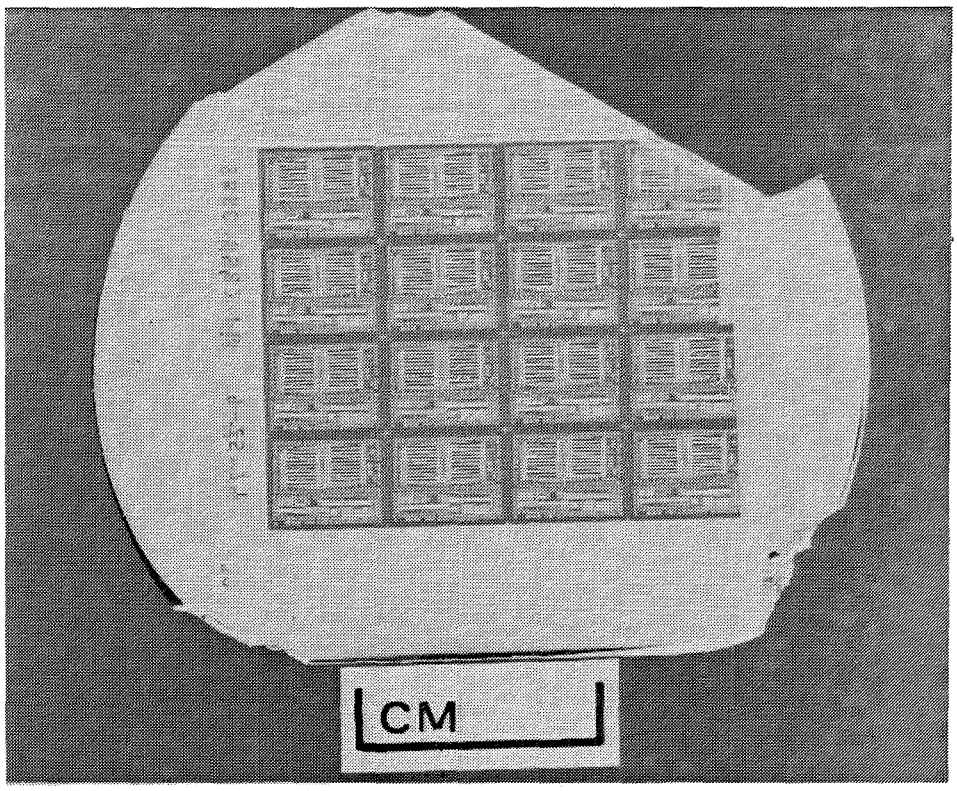
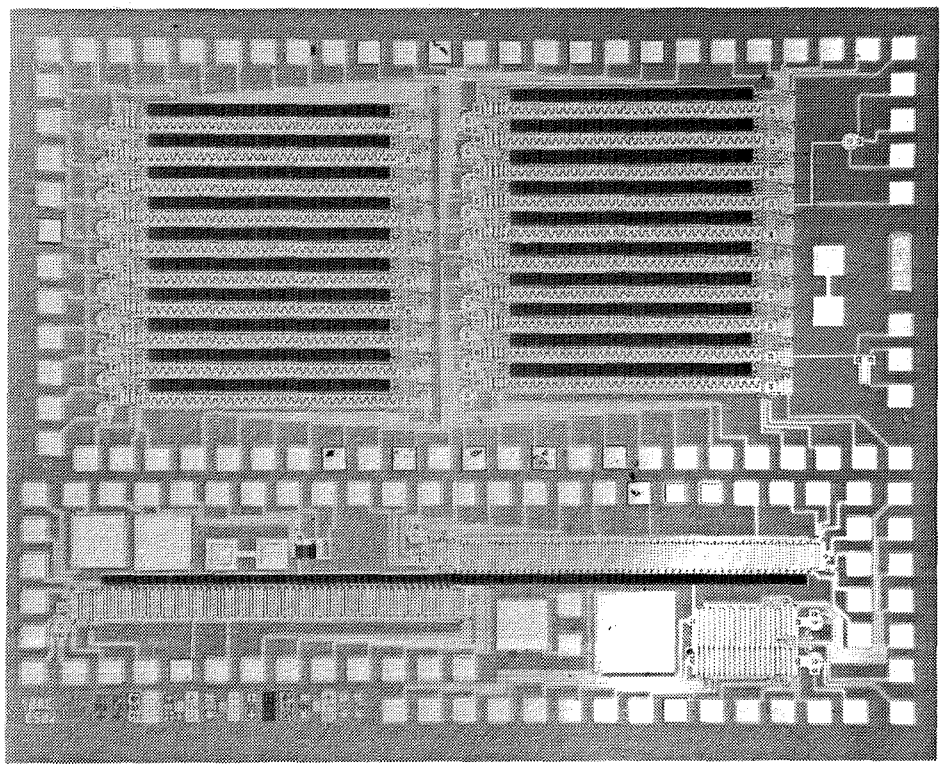


(a) InSb Wafer with Completed SBRC 8587 Chips



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(b) Completed SBRC 8587 Chip

Figure 4. InSb SBRC 8587 CCIRID (Wafer: IS558-49)

3. deposit a SiO_2 gate oxide over the thin InSb natural oxide by a low-temperature chemical vapor deposition (LTCVD) process which does not chemically or physically degrade the passivating thin natural oxide; i.e., which is benign.

Two CVD system configurations have previously been utilized for depositing benign CVD SiO_2 gate isulators. The deposition means include horizontal-flow (HCVD) and vertical-flow (VCVD) reactor geometries. These two reactors were found to produce markedly different MOS electrical characteristics on InSb. The explanation for these differences has been hypothesized to be related to the degree of homogeneous versus heterogeneous CVD reactions which take place and is totally dependent on reactor type.

In the HCVD reactor (an AMS 2600) the silane and oxygen are premixed upstream from the reaction chamber and the gas mixture flows horizontally over the wafer(s). The silane-oxygen reaction is largely homogeneous (i.e., occurs in the gas phase), with the result that SiO_2 particulates essentially precipitate onto the wafer. The resulting SiO_2 layer is benign in that it does not significantly alter the interface characteristics resulting in low N_{SS} (i.e., $N_{SS} < 10^{10}$ cm^{-2}-eV^{-1})[8,9,10] and results in little or no hysteresis as determined through capacitance-voltage (C-V) measurements and computer analysis. It was initially believed that CCIRIDs fabricated with such an insulator should have been capable of operating with CTE values approaching 0.9995 or better. However, the homogeneous nature of the CVD reaction leads to a physically granular SiO_2 film which has been found to induce lateral nonuniformities in surface potential, and give rise to a charge trapping mechanism similar in effect to, but totally distinct from, surface-state trapping. This lateral nonuniformity in surface potential has been found to be the dominating factor in limiting the charge transfer efficiency of the InSb CCIRIDs.[11]

In the VCVD reactor (an AMS 1000), the reaction volume for reactant gas intermixing is very small, with the silane and oxygen flowing vertically downward through isolated passages and impinging onto the wafer surface. The result is believed to be a largely heterogeneous reaction, where the silane, oxygen and various intermediate reaction products interact on the surface of the InSb wafer. Electrically, the InSb MOS characteristics with the vertical-flow CVD SiO_2 are poor, with high surface state density and larger hysteresis in the C-V curves. Some evidence has been obtained that VCVD SiO_2 layers are less granular than HCVD SiO_2 layers, although continued SEM studies indicate the differences are less significant than originally indicated.

It became necessary to determine whether any deposition method or system geometry could be found which simultaneously could produce considerably less-granular, denser SiO_2 layers (thus minimizing the lateral nonuniformity transfer inefficiency mechanism) while preserving the passivating properties and maintaining the N_{SS} and negligible hysteresis qualities of the thin natural oxide. Results obtained on IR&D studies during late 1979 and early 1980 indicated that these requirements could be met through the use of plasma-enhanced chemical vapor deposited (PECVD) SiO_2.

MIS samples fabricated on InSb utilizing PECVD SiO_2 have resulted in N_{SS} values $\leq 10^{11}$ cm^{-2}-eV^{-1} with negligible hysteresis. Most importantly, the granularity seen in LTCVD films is absent in PECVD SiO_2 films. In addition, MIS samples fabricated on liquid phase epitaxially grown (LPE) InSb layers have resulted in storage times ranging up to 22 seconds.

Although these results were quite significant, concern over the oxide uniformity and repeatability remained. Further investigations of these characteristics were carried out as a major task of the present contract.

The primary objective of the present contract was to fabricate a gate oxide with the electrical and physical properties necessary to achieve InSb CCIRIDs with a CTE $\geq$ 0.999 and achieve improved performance as compared to InSb imagers previously fabricated and delivered to NASA. The basic technical approach was to utilize the PECVD SiO_2 process to reduce or eliminate the physical granularity of the gate oxide films, which had been correlated with the lower than desired CTEs of the earlier-delivered imaging devices. This approach was supplemented later in the effort by investigations of horizontal CVD (HCVD) with the addition of HCl gas, an in-house HCVD AMS 2600 system process, and a third SBRC SiO_2 system process. The remainder of this report discusses the results of these MIS investigations and their impact on achieving the desired CTE result. The report is organized as follows:

1. Section 2 discusses the results obtained from investigations of oxides deposited using the PECVD SiO_2 process;
2. Section 3 discusses the results obtained from investigations of oxides deposited with the HCVD with added HCl gas process;
3. Section 4 discusses the results obtained from investigations of oxides formed with the SBRC HCVD reactor;
4. Section 5 discusses the results obtained from investigations of oxides deposited with the third SBRC SiO_2 process; and
5. Section 6 summarizes the results achieved during the contract.

Identification of commercial products in this report is to adequately describe the materials and does not constitute official endorsement, expressed or implied, of such products or manufacturers by the National Aeronautics and Space Administration.

ACKNOWLEDGMENT

The following employees of the IRC Research and Development Department are acknowledged for their contributions to this program: H.P. Bevans, M. Ray, and A.E. Sims for device process development; D.R. Rhiger for SiO_2 development; and V.A. Cotton for characterization and development of the SBRC CVD SiO_2

Special thanks are extended to C.P. Bentley and S.C. Brown for preparation of the monthly reports; and to the Publications Department for their aid in preparing viewgraphs for oral reviews and preparation of this final report.

Finally, the continued support of H.D. Hendricks and W.E. Miller of NASA LRC is acknowledged.

Section 2

MIS DEVICE FABRICATION AND CHARACTERIZATION OF PECVD SiO_2 ON InSb

The basic approach for surface passivation and fabrication of MIS devices on InSb, as described in Section 1, is based on theoretical arguments and has grown out of IR&D research dating back to 1977. A flow diagram showing the basic InSb MIS process sequence is shown in Figure 5. A schematic of the related MIS structure is shown in Figure 6.

The basic MIS process is complex in that several of the operations require critical etching steps which are subject to contamination problems. These can be limited with good control of the etchants and industrial rinse water used. A pre-deposition ellipsometric test is used as a control point to ensure that the InSb wafer surface is clean prior to passivation. The process and device characterization have been analyzed and reported by Langan[12] and Thom, et al.[13]

The previously used, pyrolytic CVD SiO_2 (HCVD and VCVD) deposition processes required several parameters to be empirically evaluated and controlled to ensure reasonable repetition in physical and electrical oxide quality. These variables included: temperature, silane (SiH_4) and oxygen (O_2) gas flow rates, and time of deposition. Investigations of the necessary operating parameters for producing quality oxides with the PECVD SiO_2 reactor revealed several new parameters which required evaluation and control before an established process could be realized.

The PECVD system is an LFE Corporation Model PND-301. A photograph and schematic view of the reactor are shown in Figures 7 and 8. Initial studies of the deposited oxide quality were carried out at the Hughes Research Laboratory in Malibu, California, but to pursue the approach further, a system was purchased from LFE Corporation in late 1979. The reactor consists of a 7.62-cm (3-inch) diameter heated wafer holder contained in a small vacuum bell jar. Silane (SiH_4), diluted in argon, is admitted through a dispensing showerhead. Nitrous oxide (N_2O) is admitted at the top of the bell jar to serve as an oxidant. The reactant gases are excited by an inductively-coupled magnetic field which surrounds the reacting chamber. The activated gases then react to form SiO_2 which is deposited on the wafer surface.

A listing of the variable parameters requiring empirical evaluation, and the ranges evaluated are shown in Table 1. In addition to the parameters shown

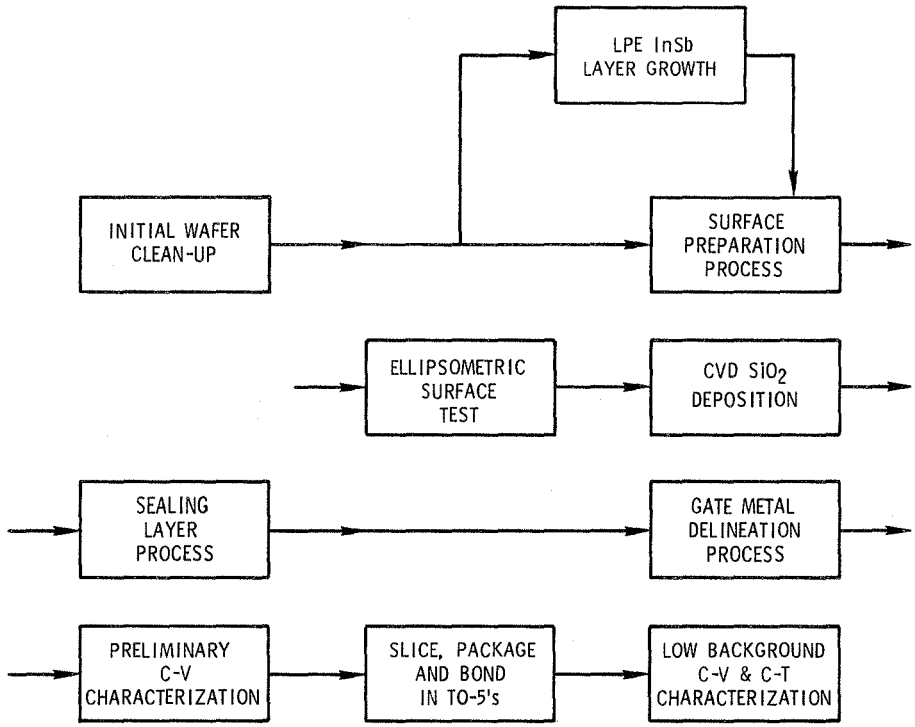


Figure 5. InSb MIS Device Process Flow Diagram

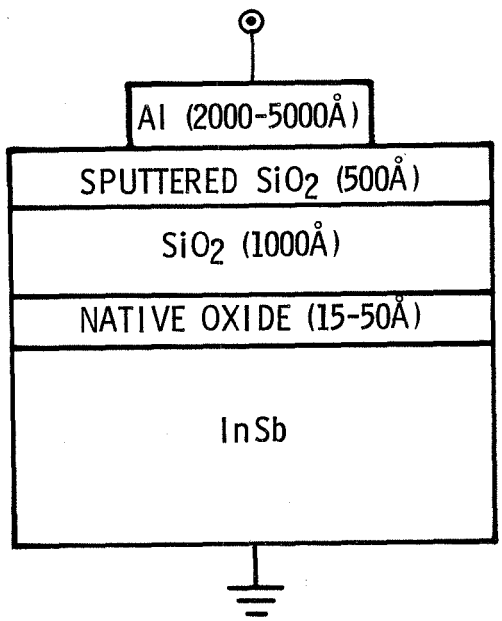


Figure 6. Schematic Cross Section of InSb MIS Structure

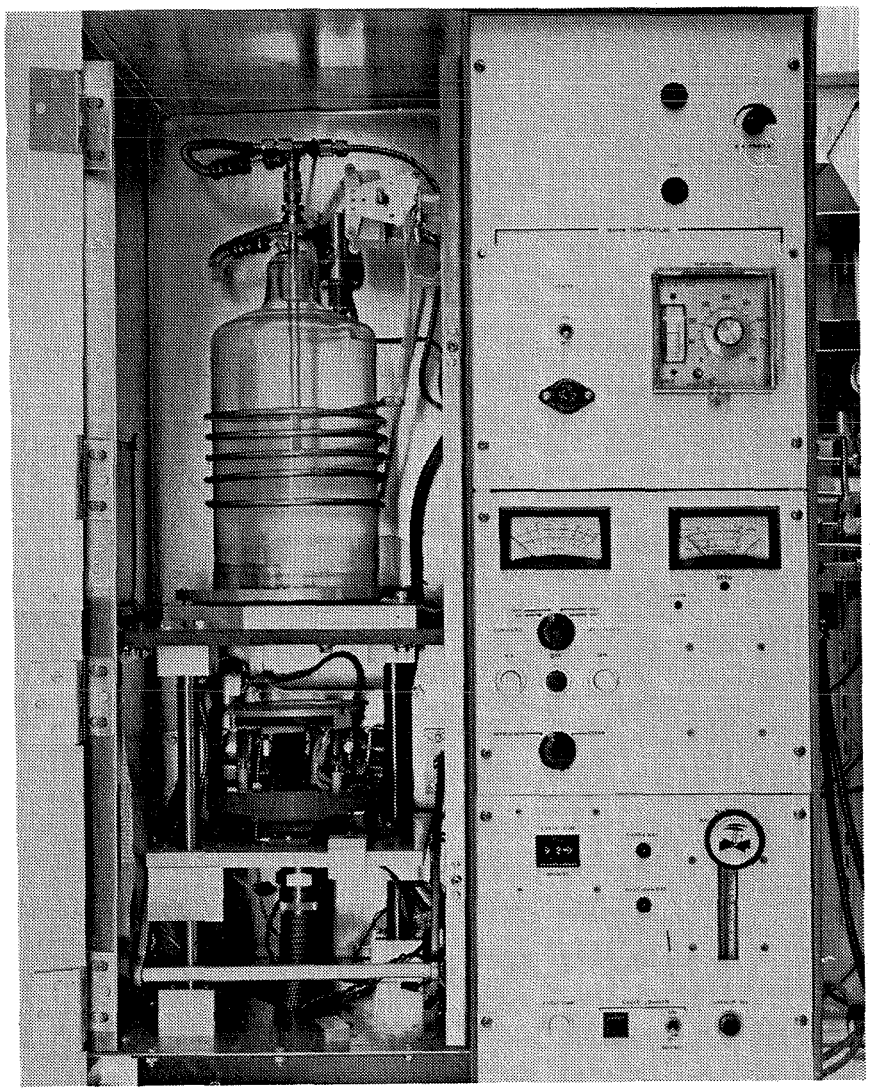


Figure 7. LFE Model PND-301 Plasma Deposition System

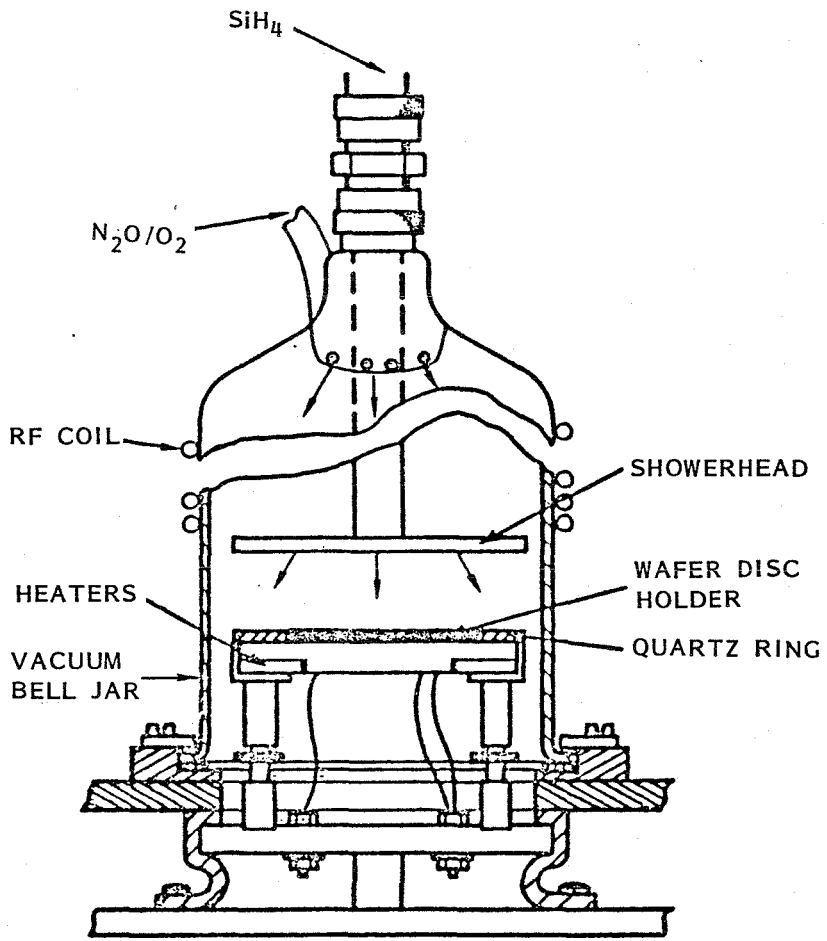


Figure 8. Model PND-301 Schematic

TABLE 1. PND-301 PECVD SiO_2 DEPOSITION PARAMETERS FOR InSb

Item	Variable Parameter	Evaluation Range	
		SI Units	Actual Units
1	Substrate Temperature	20°-250°C	---
2	RF Power	0-150 watts	---
3	Pressure with SiH_4	6.67-17.33 Pa	50-130 mTorr
4	Pressure with SiH_4 + N_2O	12.00-33.99 Pa	90-255 mTorr
5	Showerhead Height (Above Sample)	1.27-10.16 cm	0.50-4.00 inches
6	RF Coil Height (Above Sample)	8.26-18.42 cm	3.25-7.25 inches

both N_2O and O_2 could be used as oxidizing gases (N_2O preferred) and the sequence in which the gases were admitted to the chamber could be interchanged (although the system was set up to automatically inject SiH_4 first). The final parameter (one which proved to be major) was the type of showerhead used. An aluminum showerhead was included as the standard unit with the system, but SBRC [and Hughes Research Laboratories (HRL), Malibu] also purchased an optional quartz dispensing head.

Initial investigations were performed with the standard metal showerhead and involved varying the first four parameters of Table 1. Typical high-frequency (HF) and quasi-static (QS) low-frequency C-V, and conductance-voltage (G-V) characteristics from these tests are shown in Figure 9. A major improvement in these characteristics was seen upon switching to the quartz showerhead

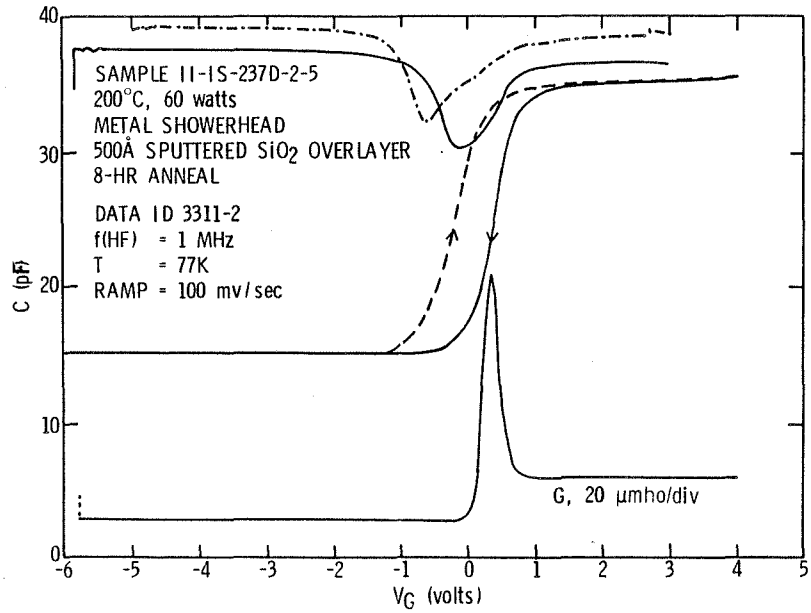
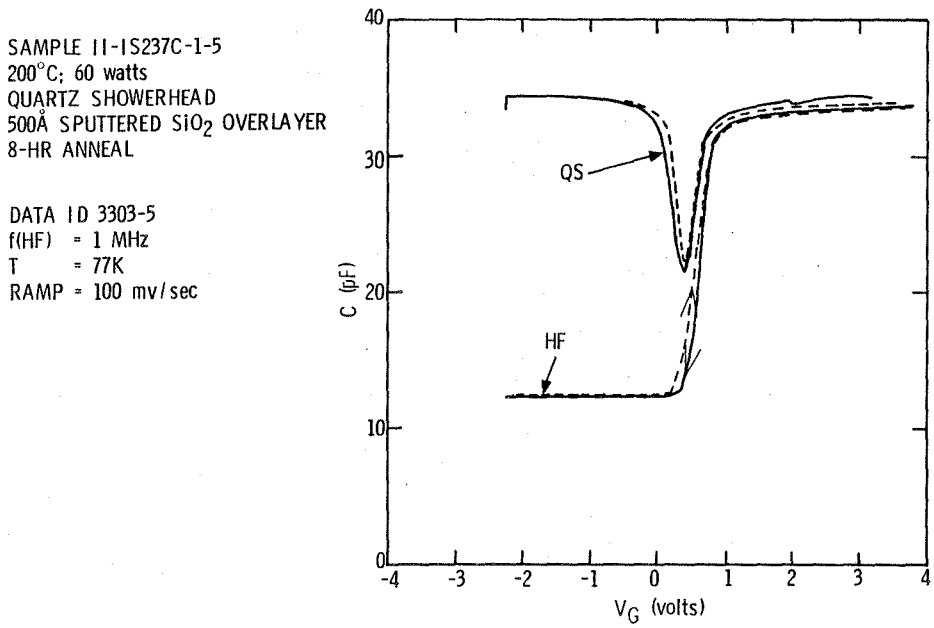


Figure 9. High-Frequency and Quasi-Static C-V Curves for PECVD SiO_2 InSb MIS Sample Using Metal Showerhead

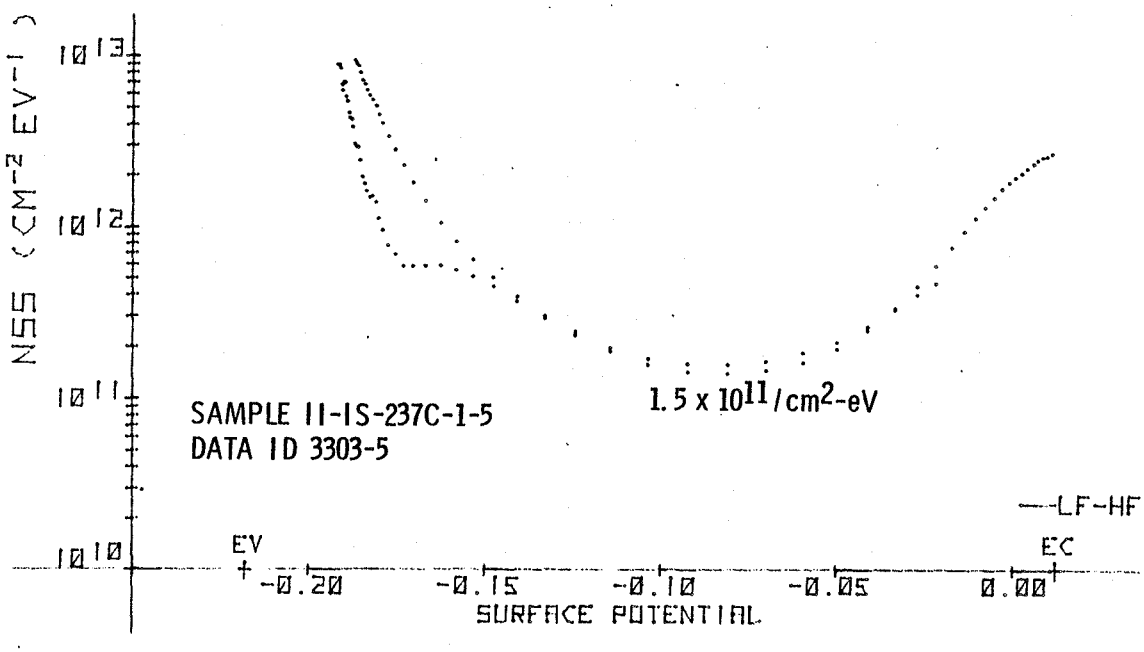
The initial test of the quartz showerhead used the best of the parameters determined from tests performed with the metal showerhead without attempting to optimize them further. Figures 10(a) and (b) show the HF and QS C-V and surface state density (N_{SS}) curves obtained from the initial trial on InSb. In addition, storage time (T_S) measurements of these MIS devices (which were fabricated on LPE InSb layers grown on bulk InSb wafers) yielded values ranging up to 22 seconds. The storage time was found to be basically bulk dominated by Zerbst[14] analysis. Beyond the electrical characteristics, scanning electron microscopy (SEM) examination of the PECVD SiO_2 surface indicated the oxide was generally nongranular in nature as shown in Figure 11.

These results were quite significant and indicated that a gate insulator which would ultimately yield the desired CTE values in CCIRIDs could be achieved. The one remaining point of major concern was related to the uniformity of the oxide deposited with the quartz showerhead. As shown in Figure 12, a three-to-one thickness variation occurred across the wafer surface. Variation to this degree is unacceptable for CCIRID processing. Therefore, further investigations were required to determine the operating parameters which would yield both good electrical characteristics and uniform thickness. The major task of the present contract was established with the intention of pursuing several investigations in which different variables would be addressed in an attempt to improve on the original results. Initially, tests were performed in an attempt to repeat the original good results. These efforts were totally unsuccessful indicating that one or more system variable(s), key to the successful deposition, was/were not precisely known.

A major problem confronted was a tendency for the system to generate vacuum leaks. In conjunction with suggestions from personnel at HRL Malibu, and our own findings, several changes were made to the system gas lines to improve the vacuum integrity and flow rate control. An initial experiment (80-IX-13) was set up to reestablish the proper flow rates and pressure in the chamber of the plasma deposition system after calibrating the capacitance manometer and performing the necessary repairs. It is reasonable to assume that, after several repairs and a long period of time, operational conditions could have changed. Also, these pressure experiments were performed earlier with the aluminum showerhead but were never done with the quartz showerhead because of the early good result. The experiment is summarized in Table 2.



(a) High-Frequency and Quasi-Static C-V Curves



(b) Surface-State Density by Quasi-Static Method

Figure 10. Measured and Calculated C-V Characteristics for PECVD SiO_2 on LPE InSb Using Quartz Showerhead

Showerhead:	Quartz
Temperature:	200°C
RF Power:	60 watts
Total Pressure:	26.66 Pa (200 mTorr)
O/S (Pressure):	0.82
Showerhead Height:	2.2 cm
RF Coil Height:	10.8 cm

1000Å PECVD SiO_2 + 500Å
RF Sputtered SiO_2

Visible Grains: 1000Å Diameter
Base Layer: Nongranular

80-12-11

Figure 11. PECVD SiO_2 Granularity for InSb Sample: II-IS 237C

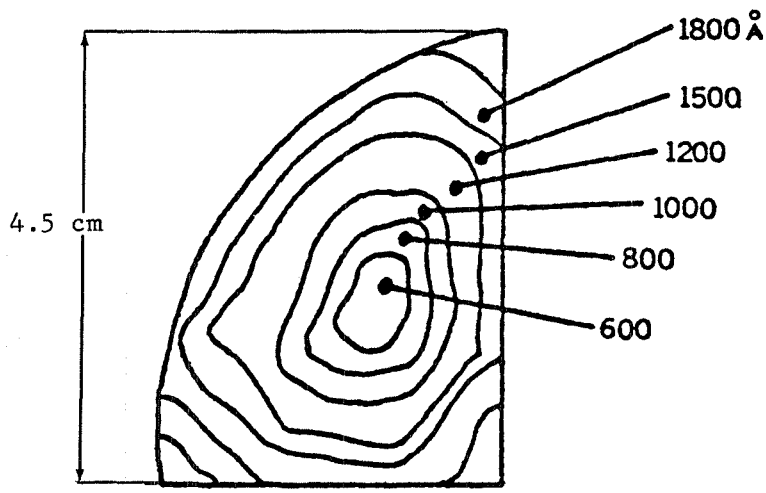


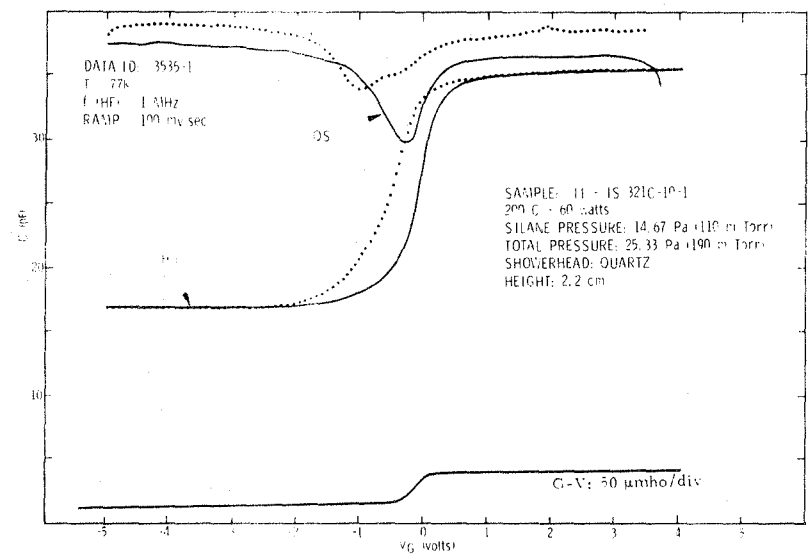
Figure 12. Illustration Showing Oxide Thickness Variation over a Wafer Surface Resulting from the Deposition Parameters Used for the Device in Figures 10 and 11

TABLE 2. EXPERIMENT 80-1X-13

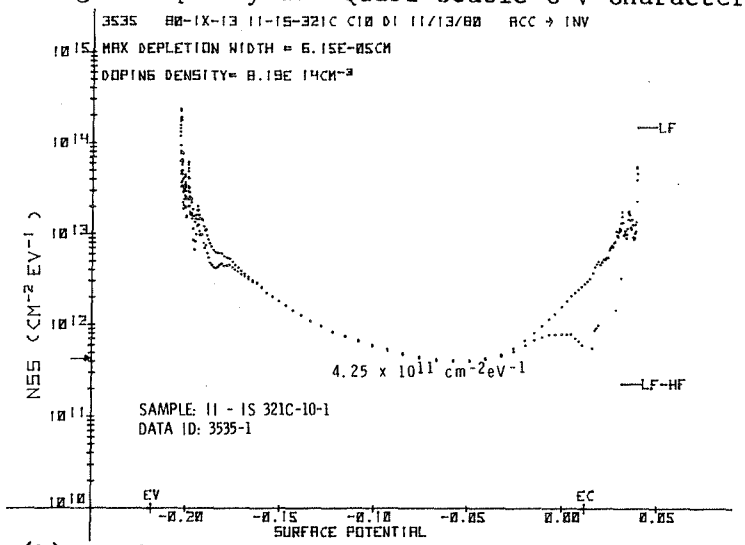
Group	SiH_4 Pressure Pa (mTorr)	Total Pressure Pa (mTorr)	N_2O Flow Rate (SCCM)
I	6.65 (50) to 17.33 (130)	25.33 (190)	---
II	8.40 (63) to 12.00 (90)	18.66 (140) to 26.66 (200)	---
III	10.66 (80)	15.20 (114) to 18.79 (141)	100 to 200

Group I in this study varied the silane and N_2O partial pressure while maintaining the total pressure constant at 25.33 Pa (190 mTorr). From the test results, the optimum partial silane pressure in this group was determined to be between 12.00 and 14.67 Pa (90 and 110 mTorr). This is in the same regime where the earlier good sample (II-IS 237C) was deposited [i.e., 11.86 Pa (89 mTorr) of silane pressure]. Figure 13(a) shows the HF, QS and G-V curves for the sample with the best characteristics from this test series. This device (II-IS 321C-10-1) has a flatband voltage (V_{FB}) which is near 0.01 volt and a fixed charge density (Q_{FC}) of ~2.0 x 10^9 charges cm^{-2}. The G-V characteristic has no loss peak present (such as the peak in the G-V curve of Figure 9) indicative of a very dense oxide. Midband N_{SS} for this sample was calculated to be 4.25 x 10^{11} cm^{-2}-eV^{-1} as shown in Figure 13(b). The density of the oxide is further represented by the current-voltage (I-V) characteristic shown in Figure 13(c) which shows $<<10^{-13}$ amp leakage at a bias of ±10 volts. The storage time for this sample was measured to have a 90% value of 4.25 sec (Figure 14). A Zerbst analysis was performed on the capacitance-transient (C-t) of Figure 14. From the Zerbst plot, the minority carrier generation lifetime (τ_g') of this sample was calculated to be 5.83 μsec and the surface recombination velocity (S) was calculated to be 0.5 $cm\text{-}sec^{-1}$. The plots for these calculations have linear regions indicative of bulk dominated samples. A SEM comparison was performed between the oxide granularity of the above device and a thermally grown SiO_2 layer on silicon which indicates the PECVD SiO_2 film is nongranular and virtually identical to the thermally grown oxide as shown in Figure 15.

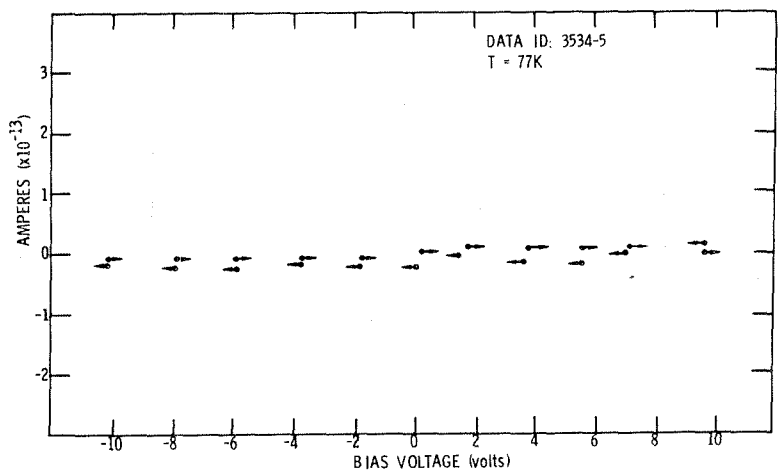
Although this sample does show some good characteristics, it has considerable hysteresis and a higher than desired N_{SS}. Neither is as low as results obtained from the (granular) HCVD process or as low as that displayed by



(a) High-Frequency and Quasi-Static C-V Characteristics



(b) Surface State Density by Quasi-Static Method



(c) Current-Voltage Response Oxide Leakage Test

Figure 13. C-V, Surface State Density and I-V Characteristics for PECVD SiO_2 on LPE InSb from Test Series 80-IX-13

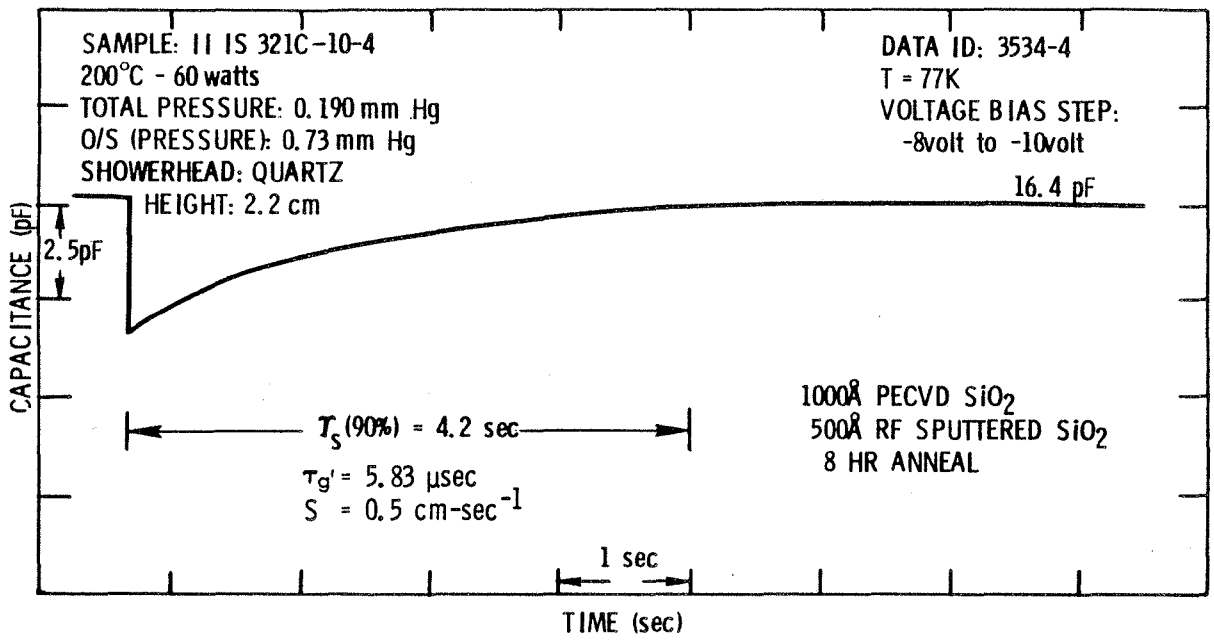
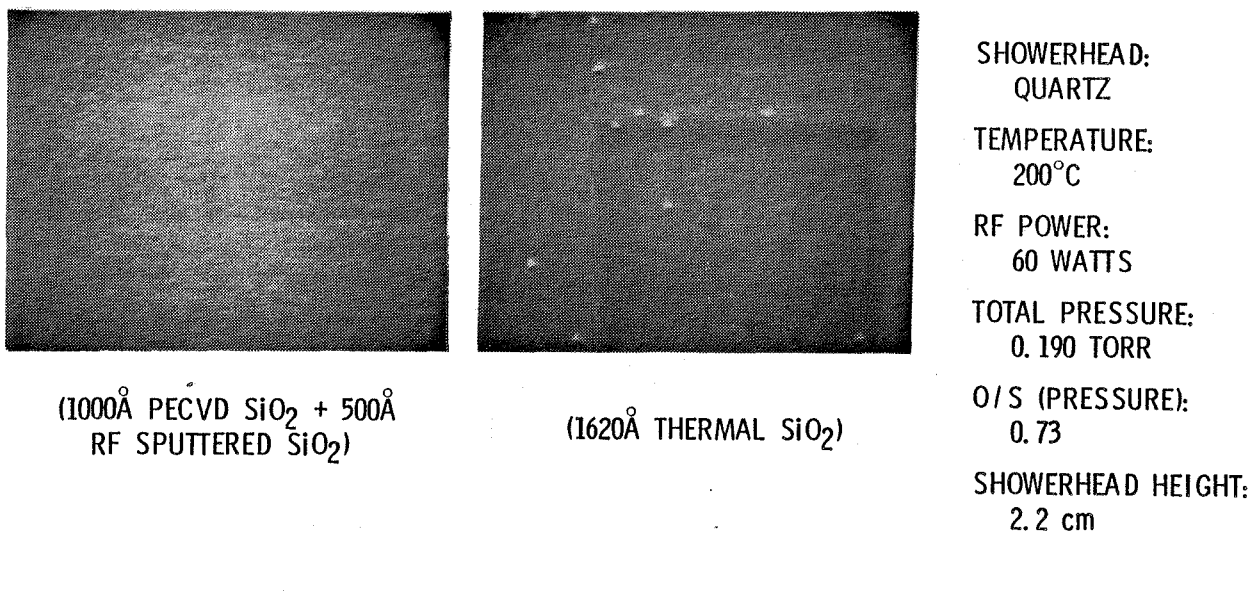


Figure 14. Capacitance-Time Response for Plasma Deposited SiO_2 on InSb



80-12-10

Figure 15. SEM Comparison of Oxide Granularity Between PECVD SiO_2 and Thermally Grown SiO_2

II-IS 237C. Significantly, the oxides so produced do lack the granularity that plagued the HCVD films used in the earlier CCDs, which was the motivation for pursuing the PECVD process.

The other samples in Group I had C-V characteristics that were degraded as the silane pressure was either increased or decreased from the optimum of 14.67 Pa (110 mTorr). In addition, the oxide uniformity became even more nonuniform than in Figure 12 and also became granular with a mean diameter of ~0.125 μm.

The Group II samples were coated by holding the silane/oxidant (SiH_4/N_2O) ratio constant at 0.45 while the total pressure was varied. In Group III sample depositions, the silane pressure was held constant, while the N_2O pressure was varied. For this group, the N_2O flow rate was measured with a newly installed mass flow meter in the N_2O line. All other variables — showerhead height, RF power, RF coil height, and temperature — were held constant and at those settings associated with the earlier good results. Within the ranges investigated for these two groups, no observable relationships between C-V quality and pressure or flow settings were realized.

RF COIL HEIGHT EXPERIMENT (80-IX-14)

The purpose of this experiment was to determine the optimum RF coil height for the PND-301 system. The coil height is not fixed and can be easily moved up and down the bell jar. It was hypothesized that during earlier tests, the coil position had not been accurately controlled and movement may have had a degrading effect on the results, or that the optimum position had not yet been established.

Four depositions were performed with coil heights of 8.26 cm (3.25 inches) (as measured from the bottom of the lowest turn to the baseplate), 10.80 cm (4.25 inches), 13.34 cm (5.25 inches), and 18.42 cm (7.25 inches). All other parameters were held constant at the settings listed in Table 3.

TABLE 3. PECVD SiO_2 PARAMETERS FOR COIL HEIGHT EXPERIMENT

Parameter	Setting
SiH_4 Pressure	10.67 Pa (80 mTorr)
Total Pressure	17.73 Pa (133 mTorr)
N_2O Flow Rate	175 SCCM
Temperature	200°C
Power	60 watts
Quartz Showerhead Height	2.22 cm (0.875 inch)
Deposition Time	120 sec

The C-V curves associated with coil heights of 8.26, 10.80 (the previously used "standard" height) and 13.34 cm were essentially identical, with -1.0 volt $\leq V_{FB} \leq$ 0 volt and moderate hysteresis. The sample with the highest coil setting (18.42 cm) was much poorer by comparison. The C-V curves for the latter sample were very nonuniform with V_{FB}s ranging to -10 volts and hysteresis as high as 10 volts. SEM photos of the sample surfaces also showed the latter sample to be much more granular. This was as expected; i.e., the reaction became more homogeneous when it occurred higher in the bell jar.

These results are consistent with the thin native oxide model. The gas flow geometry of the deposition system is such that silane impinges directly on the hot InSb surface and is able to interact with the native oxide before reacting with N_2O in the plasma higher in the bell jar. The thermodynamics of the silane/N_2O reaction are such that they do not react at 200°C to a significant degree without the plasma discharge. When the coil is lowered the plasma is also lowered and the silane/N_2O reaction takes place at the wafer surface competing with the native oxide reaction.

ELLIPSOMETRY EVALUATION

A Gaertner L117 ellipsometer was used routinely as an in-process check to determine the extent of cleanliness of freshly etched InSb surfaces, study the effect of the plasma deposition on the native oxide, and determine SiO_2 film quality by calculating the index of refraction of a sample film deposited on silicon.

The use of the ellipsometer to evaluate the degree of InSb surface cleanliness has been previously reported by Langan.[15] In his work, cleaved <110> InSb surfaces were measured to determine the complex index of refraction

$$\hat{n}_3 = n - ik \tag{1}$$

for the thin native oxide. From these studies an effective InSb substrate index of $\hat{n}_3 = 4.36 - 1.65i$ was determined to be the cleanest surface obtainable without working in a vacuum. This complex number was associated with measurable ellipsometer readings of relative amplitude change (ψ) = 18.65 and relative phase change (Δ) = 148.60.

The values ψ and Δ are used to track the index of refraction and oxide thickness. The measured ψ and Δ values are iterated through a program, described by Loser and Larsen,[17] which was modified for use on a Hewlett-Packard MX1000 computer.

Results of the cleaved InSb study indicated that a native oxide ~15Å thick is immediately grown upon exposing the InSb surface to atmospheric conditions. Similar test results indicated the cleanest InSb surface obtainable following an etch process had a native oxide ~45Å thick and an index of refraction near 3.6. These correlate with ψ and Δ values of 19.5 and 140.8, respectively.

Significant variation from these values is indicative of a nontypical surface, usually due to contamination, and can be correlated with poor C-V results. Therefore, wafers are checked with the ellipsometer after the surface cleanup etch to determine if the wafer requires additional cleaning before proceeding with the deposition.

Ellipsometric Native Oxide Analysis

To determine the effect of a plasma discharge on the native oxide, an experiment was performed in which cleaned wafer surfaces were exposed to various phases of the plasma deposition sequence. Ellipsometric measurements were taken before and after exposure, in an attempt to detect variation in the native oxide condition.

The observed effect on an InSb wafer from a 120-second "soak" at a temperature of 200°C (under normal vacuum, no gases admitted, and the plasma left off) was a subtle change in the native oxide thickness and/or composition as indicated by the following ellipsometer readings:

1. ψ and Δ before heat exposure: 19.30; 141.50
2. ψ and Δ after heat exposure: 19.50; 140.00

This was hypothesized to be related to residual oxygen remaining in the vacuum chamber.

The effect of exposure to the plasma at 200°C (still with no gases admitted to the chamber) was predictable in that in each case substantial thickening of the native oxide was observed as shown in Table 4.

TABLE 4. EFFECTS OF PLASMA EXPOSURE ON InSb THIN NATIVE OXIDE

Power (watts)	Time (sec)	Approximate Native Oxide Thickness (Å)
20	120	70
60	120	70
100	120	85

In each case, the index of refraction decreased from 3.0 to 2.3 with no marked change in k (dispersion coefficient). It is difficult to state exactly what caused this decrease since segregation of indium and antimony can occur without the ellipsometer detecting it.

Of serious concern was the automatic deposition sequence of the reactor in which diluted silane is admitted and flows for 180 seconds prior to the plasma being ignited. Since silane is injected from the showerhead directly onto the wafer surface, it is conceivable the native oxide could be reduced, thereby degrading the interface characteristics. It should be noted, however, that the previously-produced excellent sample (II-IS-237C) utilized this very same sequence. Ellipsometric readings of the surface, after exposure to silane at 200°C for varying times, failed to show any change in its condition; i.e., ψ and Δ remained unchanged.

To further analyze this condition, an ESCA analysis was performed at the Jet Propulsion Laboratory in Pasadena, California. This analysis indicated that, after exposure to silane for 5 minutes, the native oxide (originally In_2O_3) was in a reduced form and an oxidized form of silicon was present on the wafer surface.

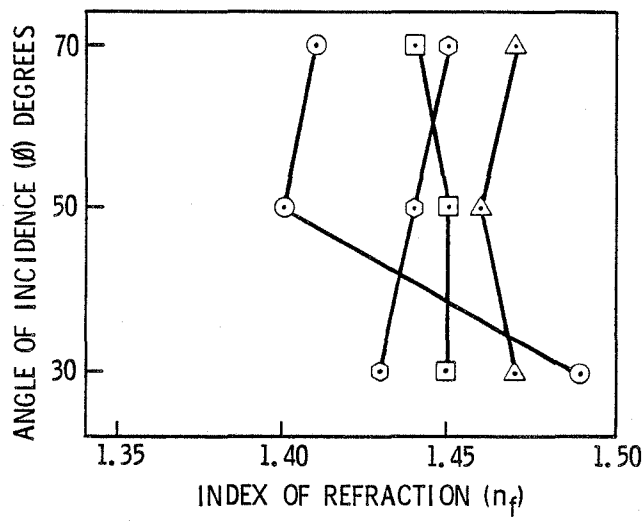
In concluding this investigation, the ellipsometer was found to be capable of detecting small changes in the thickness and refractive index of the thin native oxide. Small changes in chemical composition, however, which might markedly affect electrical characteristics, will not necessarily change the optical properties sufficiently to be detectable.

Ellipsometric Analysis of CVD SiO_2

The ellipsometer can effectively monitor the quality of deposited SiO_2 and was used to evaluate CVD SiO_2 films as deposited on silicon. One method of characterizing a thin film is to take single-point measurements using various angles of the incident beam. For a good quality oxide, the ψ and Δ values for each angle should yield the same index of refraction and thickness when the data are reduced by the computer program.

Three samples representing VCVD, HCVD, and PECVD SiO_2 films were selected for this test. The ψ and Δ values were recorded for each sample at three different incident angles (30°, 50°, and 70°). The index of refraction was obtained assuming nonabsorbing or nearly nonabsorbing films and minimizing the error.

Figure 16 shows the results of the measurements for these samples. As shown, the HCVD and VCVD oxides are typically well behaved and uniform; i.e., the calculated index does not vary greatly with ellipsometer angle. PECVD SiO_2 is similarly well behaved in certain regions of some samples, as shown by the curve labeled "good region." However, it is nonuniform over the entire wafer, and in other regions the index varies greatly with ellipsometer angle, indicating the SiO_2 has nonideal characteristics in these regions. The nonlinearity in the "nonuniform" region can perhaps be attributed to improperly assuming the film is nonabsorbing which would result in erroneous index of refraction values.



⊡= n_f VERSUS Ø FOR TYPICAL HCVD OXIDE

△= n_f VERSUS Ø FOR TYPICAL VCVD OXIDE

⊙= n_f VERSUS Ø FOR PECVD OXIDE (NON-UNIFORM REGION)

⊙= n_f VERSUS Ø FOR PECVD OXIDE (GOOD REGION)

Figure 16. Measured Index of Refraction versus Ellipsometer Angle for Various CVD SiO_2 Samples

DEPOSITION UNIFORMITY

It has been observed on large silicon wafers used as trial substrates that the refractive index varies significantly about the center of the PND-301 wafer platen. In a single deposition the index may vary from 1.36 to 1.46 as shown in Figure 17. As the refractive index is an indication of the quality of the oxide, it is important that the wafer be always placed in the best position with respect to the platen, showerhead, RF coil, etc. The quartz showerhead (Figure 18), which provides better C-V characteristics than the metal showerhead, consists of a quartz ring with several holes for gas dispersion. Since the holes were pulled by hand, the spacing and orientation are not uniform. Thus, the silane gas flow is critically dependent on the placement of the showerhead.

Because standard InSb test samples (quarter-wafers) are small (~1.3 cm × 1.3 cm), it is difficult to determine whether variations in MIS C-V data occur as a result of edge effects or real variations in the deposition system. Therefore, an experiment was performed to correlate C-V data with areas of good and poor refractive index. A full size InSb wafer (3.2-cm diameter) was placed on the platen as shown in Figure 19. The C-V data accumulated are summarized

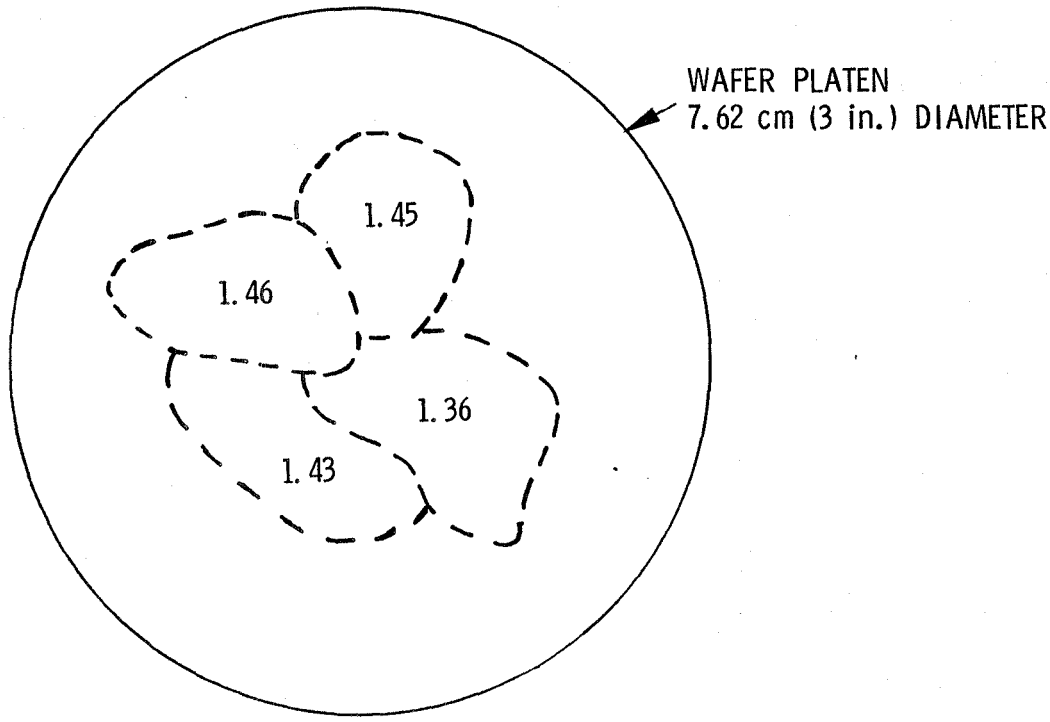


Figure 17. Variation in Index of Refraction of a Typical PECVD SiO_2 Film (Dotted lines show tendencies and are not exact)

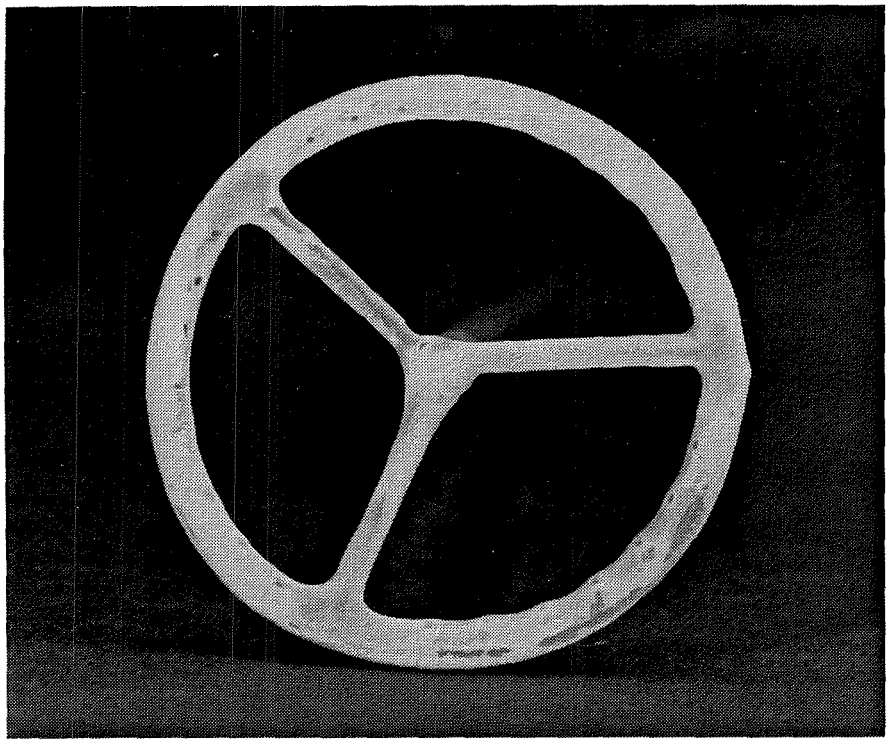


Figure 18. PND-301 PECVD System Quartz Showerhead

81-3-63

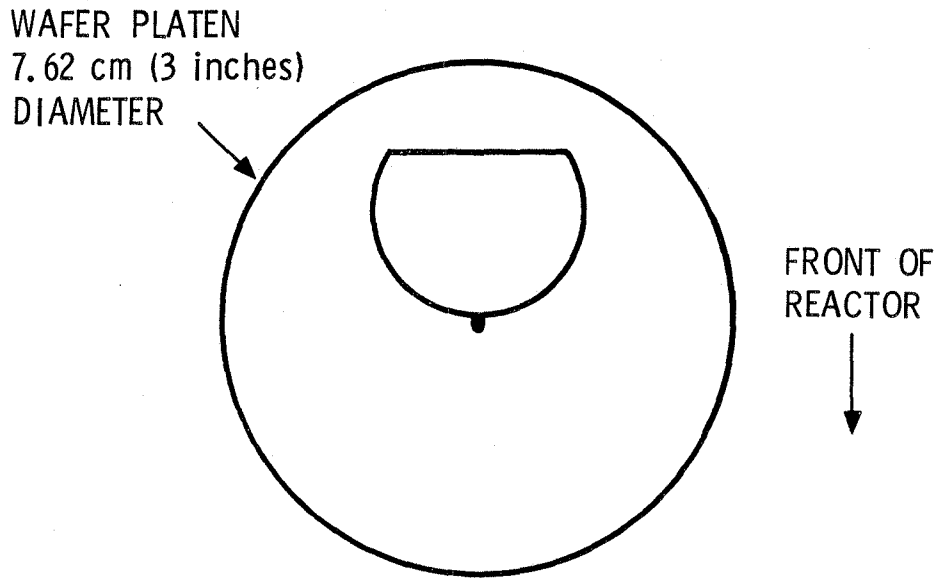


Figure 19. Position of Wafer IS 618-3 on Platen During Deposition

in Figures 20 through 24. Figure 20 shows the variation in oxide capacitance (C_{ox}) over the entire InSb wafer as measured every 2.5 mm. From the capacitance, the oxide thickness was calculated by assuming the dielectric constant (K_{ox}) to be 3.9. The variation in thickness is shown in Figure 21. The thickness values correspond well with those obtained from the actual colors of the wafer, thus the assumption of the dielectric constant is valid. The flatband voltages, V_{FB}, and fixed charge, Q_{FC}, are given in Figures 22 and 23. Figure 24 shows the variation in hysteresis. In this case, the difference in V_{FB} (forward trace minus reverse trace) was divided by the sweep width to give a normalized value.

These diagrams show a tendency for the right half of the wafer to be better than the left half, and the lower righthand corner to be the best overall, in terms of V_{FB}, Q_{FC}, and hysteresis. However, because of the extreme variation in thickness, this region is unusable for actual device fabrication. Thus, it is impractical to fabricate devices by simply placing a wafer on the "good" deposition area of the platen.

81-3-67

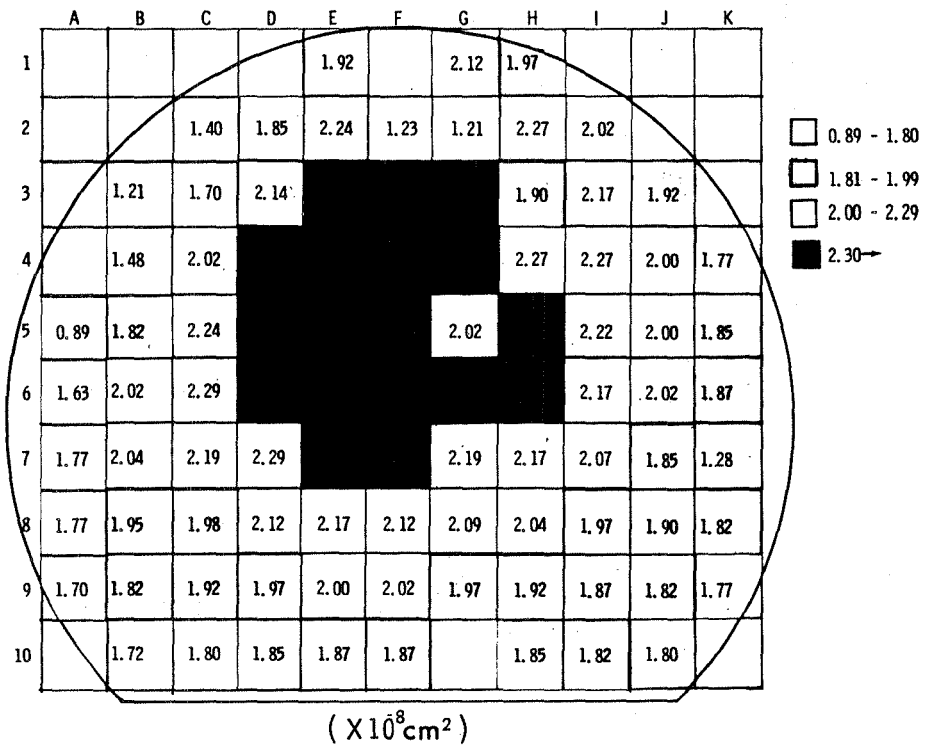


Figure 20. Oxide Capacitance (C_{ox}) for Wafer IS 618-3 (PECVD SiO_2)

81-3-70

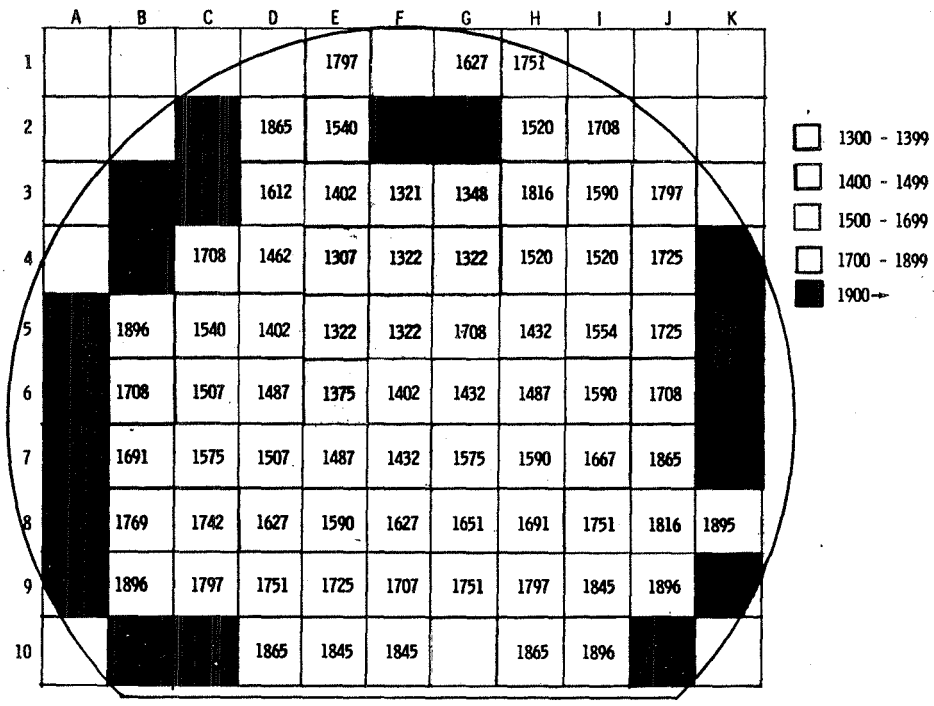


Figure 21. Variation in PECVD SiO_2 Thickness as Calculated Using a Dielectric Constant (K_{ox}) = 3.9

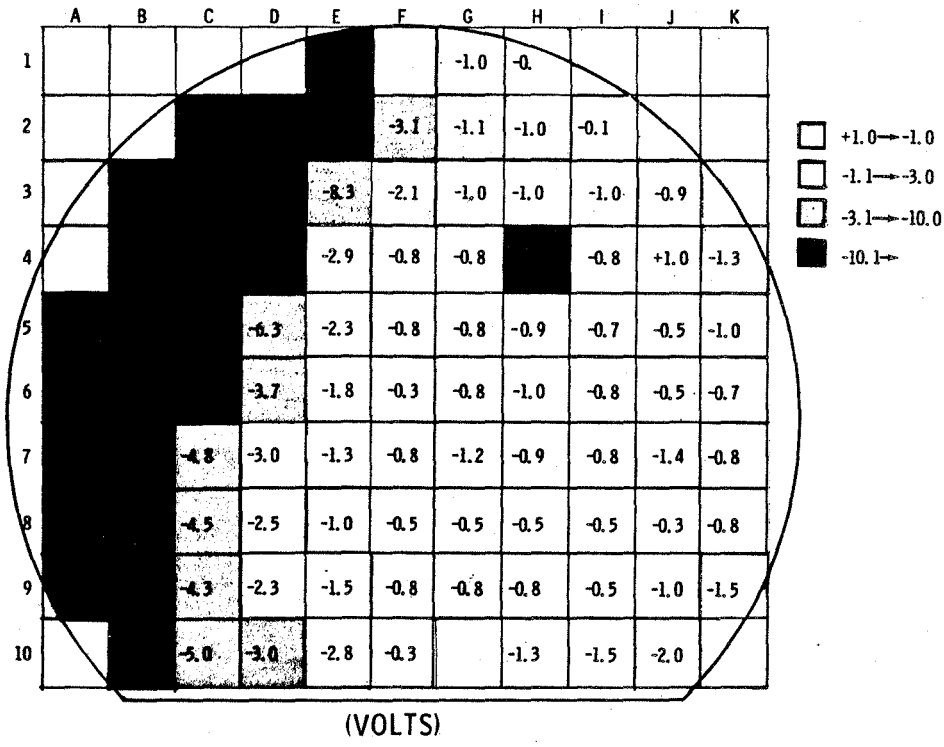


Figure 22. Measured Flatband Voltage (V_{FB}) for Wafer IS 618-3 (PECVD SiO_2)

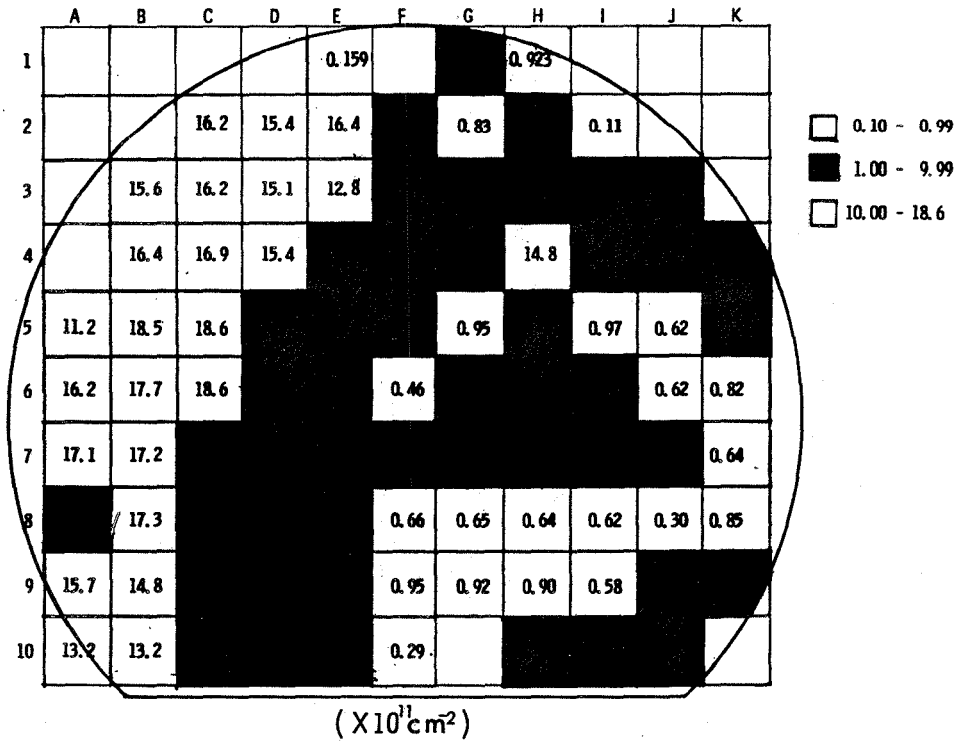


Figure 23. Fixed Charge, Q_{FC}, over Wafer IS 618-3

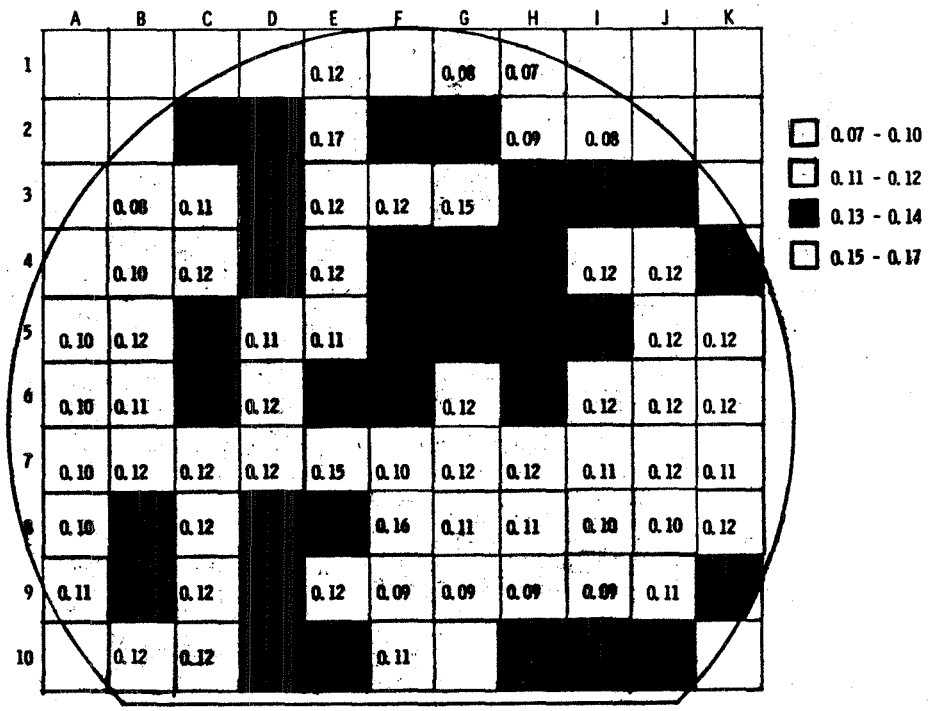


Figure 24. Normalized C-V Hysteresis ($\Delta V_{FB}/\Delta V_G$), Wafer IS 618-3

ESCA STUDY OF PECVD SiO_2 ON InSb

An experiment using ESCA, with an ion etching technique, to profile a PECVD SiO_2 sample on InSb was performed at Surface Science Laboratories in Palo Alto, California. With this technique, chemical information was obtained as a function of etch time. In a 1978 IR&D study, similar analyses were performed on InSb samples with horizontal and vertical CVD SiO_2 layers. The objective of this experiment was to gather data on the effect of plasma deposition on the SiO_2/InSb interface and to compare these results with interface results from the pyrolytic oxides studied earlier.

One of the difficulties encountered in understanding the nature of the interface resulting from plasma deposited SiO_2 stems from the inability to make direct electrical correlations. As has been established, any given deposition is nonuniform across the 7.62-cm wafer platen. Therefore, it is unreliable to deposit on two samples simultaneously (one for an MIS structure and the other for ESCA) and assume they are identical. Similarly, the deposition is not reproducible; a subsequent deposition is not necessarily the same as the first. It is also not possible to analyze testable MIS structures by ESCA, because

of thickness nonuniformities resulting from removing the metal gate. Also, the interface becomes diffuse when a thick (500Å to 1000Å) sample is analyzed. Thus, one has no assurance that a single PECVD analysis is in any way representative of a typical PECVD sample.

In spite of these difficulties, some differences and similarities between PECVD and pyrolytic CVD samples are noted.

Differences

1. Contrary to pyrolytic CVD samples, the PECVD sample did not show an Sb-rich region at the native oxide/substrate interface. Figures 25, 26, and 27 show In/Sb atom ratios as a function of etch time for all three reactors. Examining the 3d lines (which are "shallower" electrons), it can be seen in Figures 25 and 26 that the ratio drops before reaching a bulk value of about 1.3 for the pyrolytic CVD samples. The relative amount of Sb at this point is higher than in the bulk. (The bulk value of 1.3 is an artifact of the instrument and does not imply a nonstoichiometric substrate.) The PECVD sample (Figure 27) shows a slow decrease to the bulk value of 1.2 for 3d electrons.
2. There is no evidence for the presence of antimony oxides anywhere in the PECVD or vertical CVD samples as analyzed by Surface Science Laboratories. It is possible that antimony oxides were reduced by the ion beam during the analysis process. Another analysis performed on horizontally-deposited CVD samples indicated that traces of antimony oxide possibly existed at the interface. ESCA studies of VCVD and HCVD samples performed by JPL using a chemical depth profile etch technique, showed a possibility that substantial amounts of antimony oxides were present. Samples of PECVD SiO_2 on InSb were also sent to JPL for analysis but, due to scheduling and system difficulties, were not concluded.
3. Indium is present in the PECVD sample primarily in the elemental form with a small amount of oxide also detected at certain etch points. The maximum amount of oxide present is small, on the order of a few percent similar to that observed for the vertically-deposited SiO_2 and much less than observed for the horizontally-deposited sample. In each case the oxide/elemental ratio was greatest away from the interface and decreased as the interface was approached.

Similarities

1. In all three samples an In-rich region was found in the SiO_2 layer at the beginning of the interfacial region.
2. The O/Si ratios as a function of etch time are seen to decrease from a value near 2 observed in the SiO_2 to a value near 1.5 at the interface. Accompanying this deficiency is the appearance of a weak shoulder on the low binding energy side of the main Si(2p) line which may indicate the presence of a reduced form of Si.

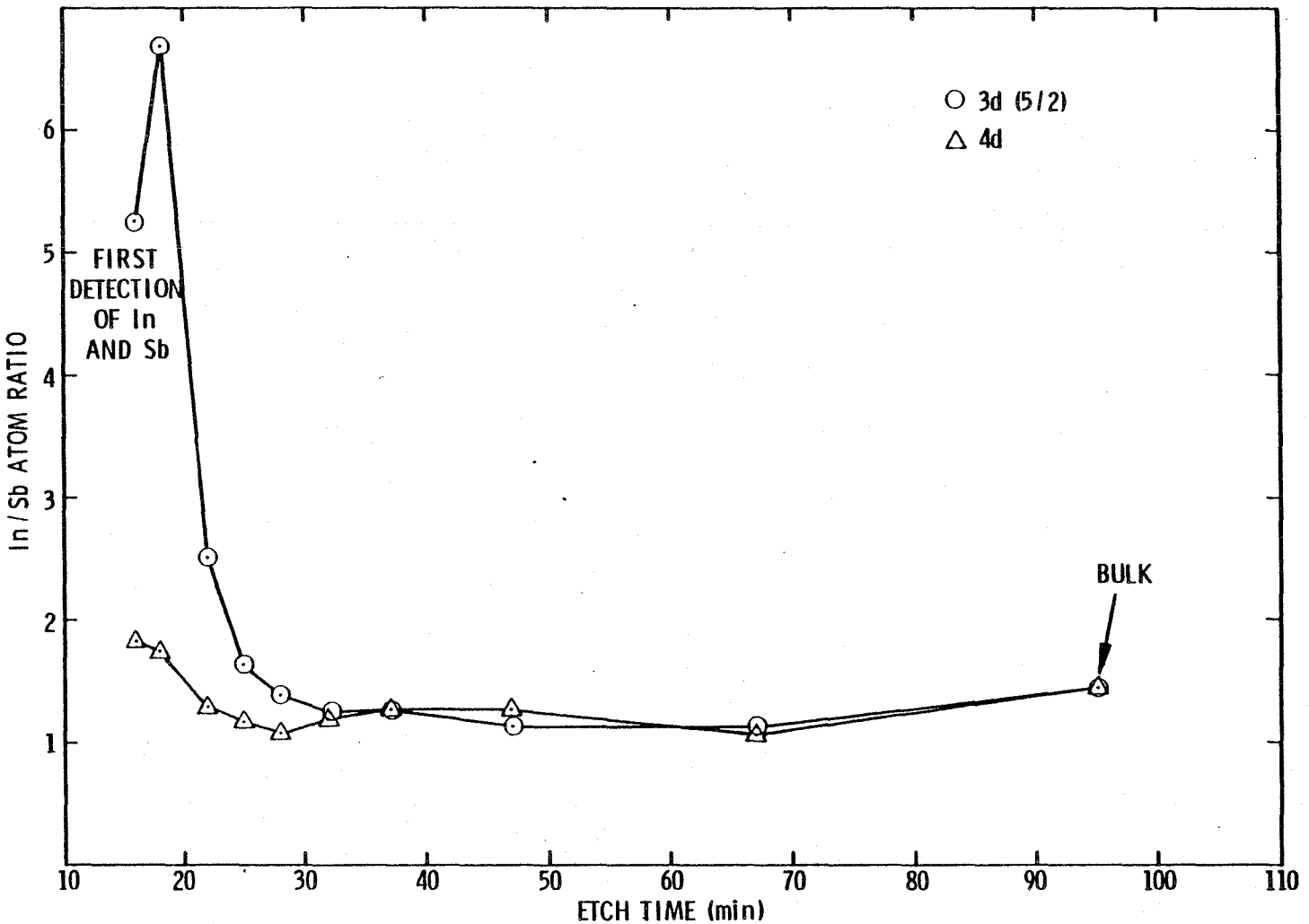


Figure 25. In/Sb Ratio as a Function of Etch Time for Vertical CVD SiO_2 Deposited on InSb

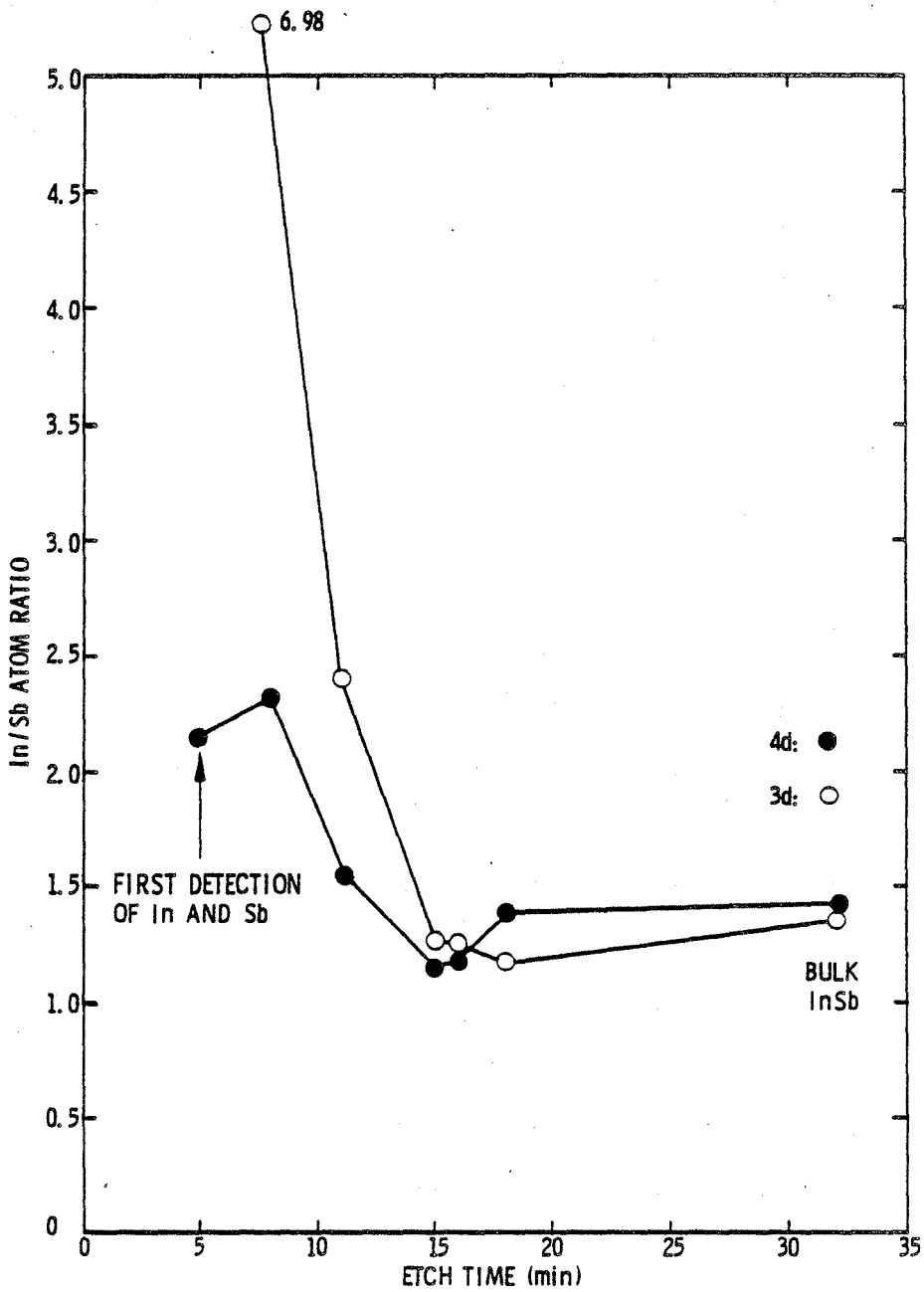


Figure 26. In/Sb Ratio as a Function of Etch Time for Horizontal CVD SiO_2 Deposited on InSb

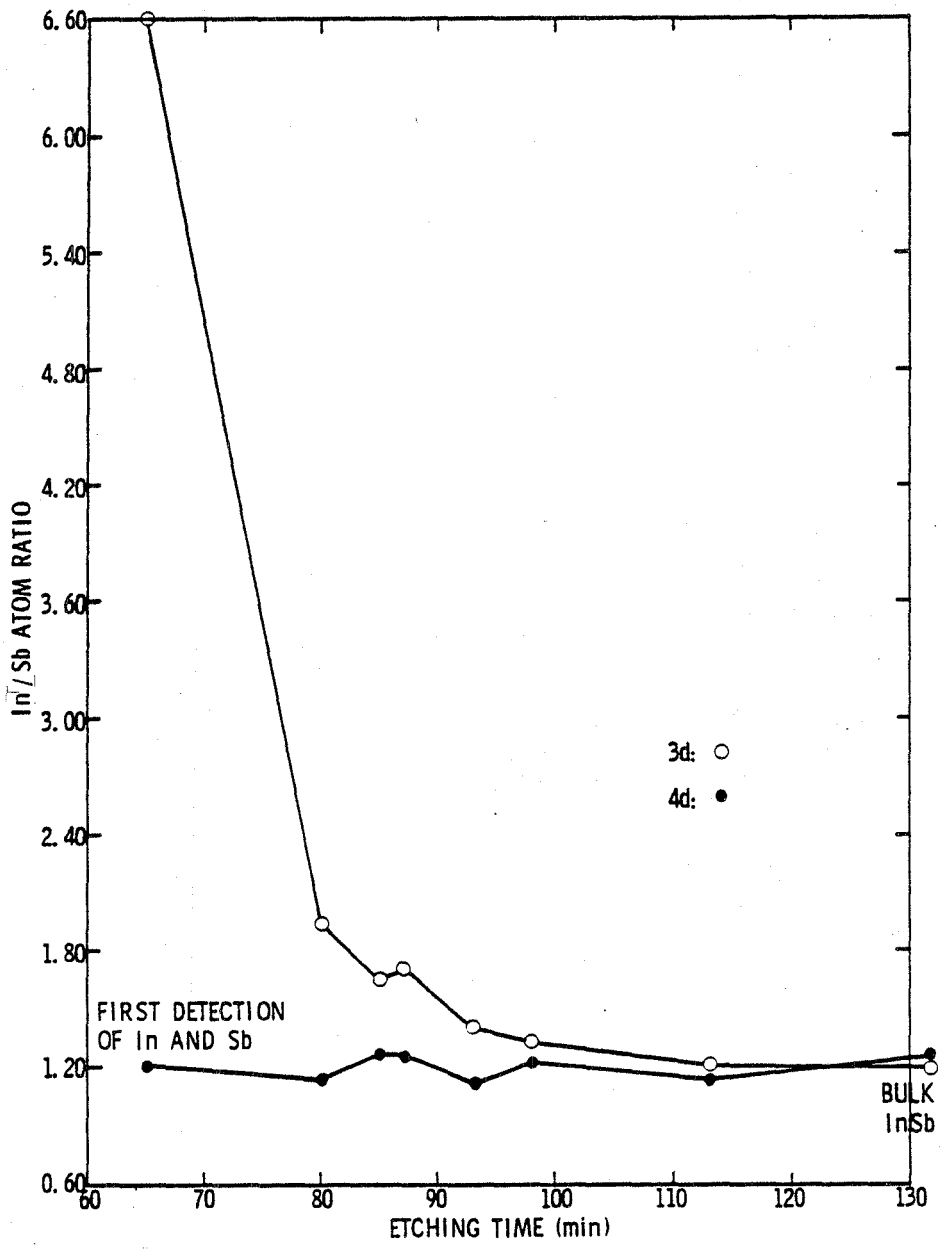


Figure 27. In/Sb Ratio as a Function of Etch Time for PECVD SiO_2 Deposited on InSb

FINAL EVALUATIONS OF PECVD SiO_2 ON InSb

From the test results that have been discussed, it is clear that the non-uniformity and repeatability of the oxide, resulting from using the quartz showerhead, must be improved before PECVD SiO_2 is useful for InSb imager fabrication. Total pressure, gas ratios, showerhead height and RF coil height have been extensively varied without substantial improvements in either uniformity or repeatability of the SiO_2 layers deposited with the quartz showerhead. There are three possible solutions to this problem:

1. modify the quartz showerhead design to disperse the silane more uniformly over the platen and reduce turbulent flow;
2. modify the system, if possible, to premix the silane with the nitrous oxide prior to or simultaneous with admission to the reaction chamber; or
3. modify the system, if possible, to rotate either the quartz showerhead (or a newly-designed dispersion head) or the platen.

Material and hardware to investigate potential solutions (1) and (2) were ordered. Quartz plates and diamond drills were received and fabrication of a new quartz showerhead (option 1), similar to the aluminum plate showerhead, was initiated. But, the contract technical period expired before assembly could be completed. Option (3) was considered to be too costly and would require a considerable outlay in capital before it could be performed. The hardware for option (2) was ordered and assembled in the reactor, and experiments were initiated prior to the end of the contract period.

A final experiment was performed following reworking the PND-301 gas lines to allow the reactant gases (SiH_4 and N_2O) to be premixed prior to being admitted into the bell jar. The mixed gases were then distributed through the showerhead. For this test, both the existing quartz and metal showerheads were used. The fundamental purpose of the experiment was to determine the effect on uniformity. In addition, one of the tests included mounting the wafer on the platen at room temperature and allowing the substrate to heat to 200°C in vacuum. (This had not been done previously because the temperature controller overshoots ~50°C unless it is very slowly increased to the set point.) For the test, the temperature was increased from 20°C to 200°C over a period of 2.52×10^3 seconds (42 minutes). Even at this rate, the temperature overshot to ~245°C.

Initially when using the quartz showerhead, the deposition nonuniformity increased with the premixed configuration. The total pressure was then reduced by one-half, keeping the gas ratios approximately the same. This resulted in an extremely uniform coating which varied only 15% over a circular area ~5 cm in diameter. The index of refraction of this SiO_2 was uniformly 1.46 and initially reproducible from run to run.

The HF and QS C-V and G-V curves showing the characteristics achieved with the quartz showerhead (heated from 25°C to 200°C under vacuum) are shown in Figure 28.

The data are encouraging in that they show a flatband voltage which is near zero and hysteresis of ~0.1 volt. Discouragingly, there is a high loss peak in the G-V curve near zero volts. Current-voltage tests of these devices yielded a 77K leakage current on the order of 5×10^{-11} amp at a bias of ±3.0 volts.

The N_{SS} for the device is shown in Figure 29 and has a minimum value of 3.6×10^{11} cm^{-1}-eV^{-1}, although the minimum is shifted from midband to within 0.083eV

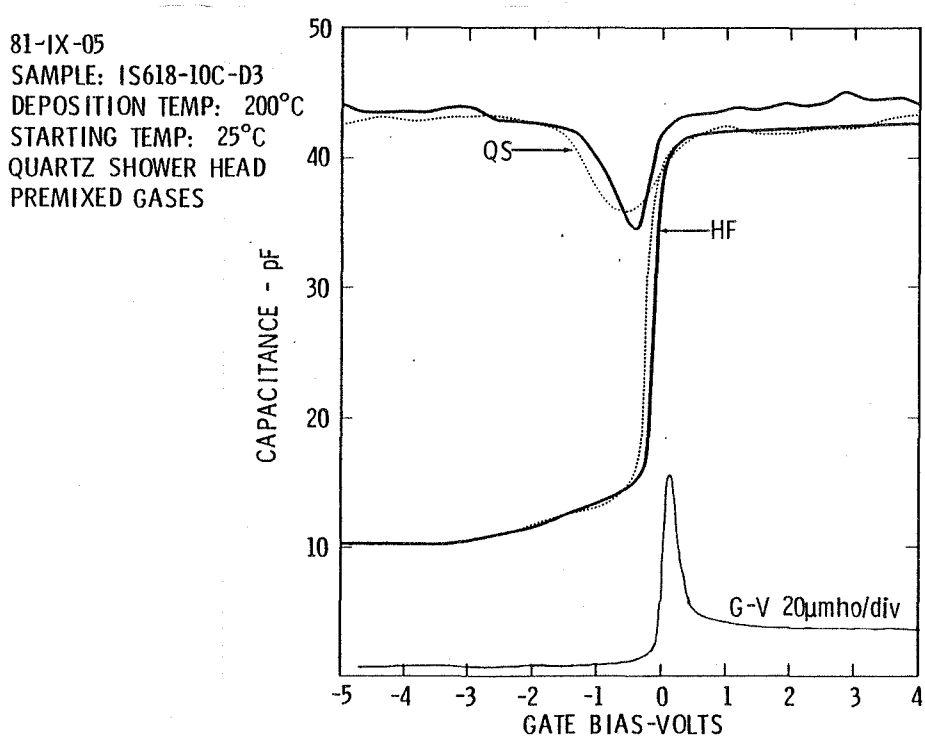


Figure 28. C-V Characteristics, PECVD SiO_2 on InSb

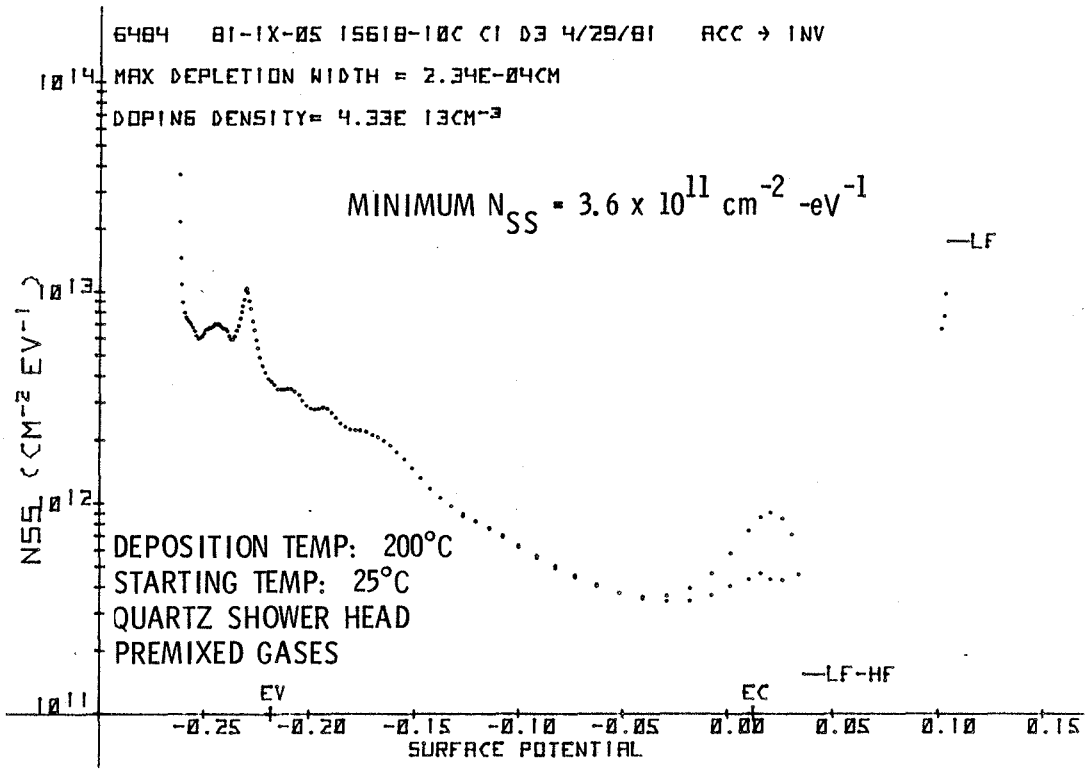


Figure 29. Surface State Density, PECVD SiO_2 on InSb

of the conductance band. SEM examinations were conducted on the various films deposited. These showed a tendency toward some granularity which was not as good as seen with the very good PECVD samples but much better than the HCVD samples.

Tests using the metal showerhead were, in general, a bit worse than with the quartz showerhead, although no optimization of either was performed.

CONCLUSIONS OF PECVD SiO_2 EVALUTION

Based on the results of the studies that have been carried out on IR&D as well as this program, it has been determined the PECVD SiO_2 deposition parameters associated with the best InSb MIS C-V characteristics are as shown in Table 5. These parameters are known to yield occasional samples with good to excellent quality. The depositions associated with these parameters are still nonuniform and nonrepeatable.

Some trends toward uniformity and repeatability improvement were seen with premixing the gases and heating the substrate under vacuum, but these deposition processes have not been optimized.

TABLE 5. PARAMETERS FOR PECVD SiO_2 DEPOSITIONS ON InSb

Parameter	Setting
Temperature	200°C
Power	60 watts
Showerhead	Quartz
Showerhead Height	2.22 cm (0.875 inch) above substrate platen
Silane Pressure	13.33 Pa (100 mTorr)
Total Pressure	26.67 Pa (200 mTorr)
RF Coil Height (Bottom Coil)	10.80 cm (4.25 inches) above base plate
Sample Position	Left and back of platen center

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Section 3

EVALUATION OF HCVD/HCl SiO_2 ON InSb MIS DEVICES

Through the introduction of a small amount of HCl in the gas stream during CVD SiO_2 deposition, some investigators have been able to significantly reduce interface states and distributed charge within the oxide.[17,18] The HF C-V results of a 1981 IR&D experiment performed at the Naval Oceans Systems Center, San Diego, are shown in Figure 30. It is clear from these trials that the presence of HCl considerably reduced the flatband voltage, hysteresis, and N_{SS}.

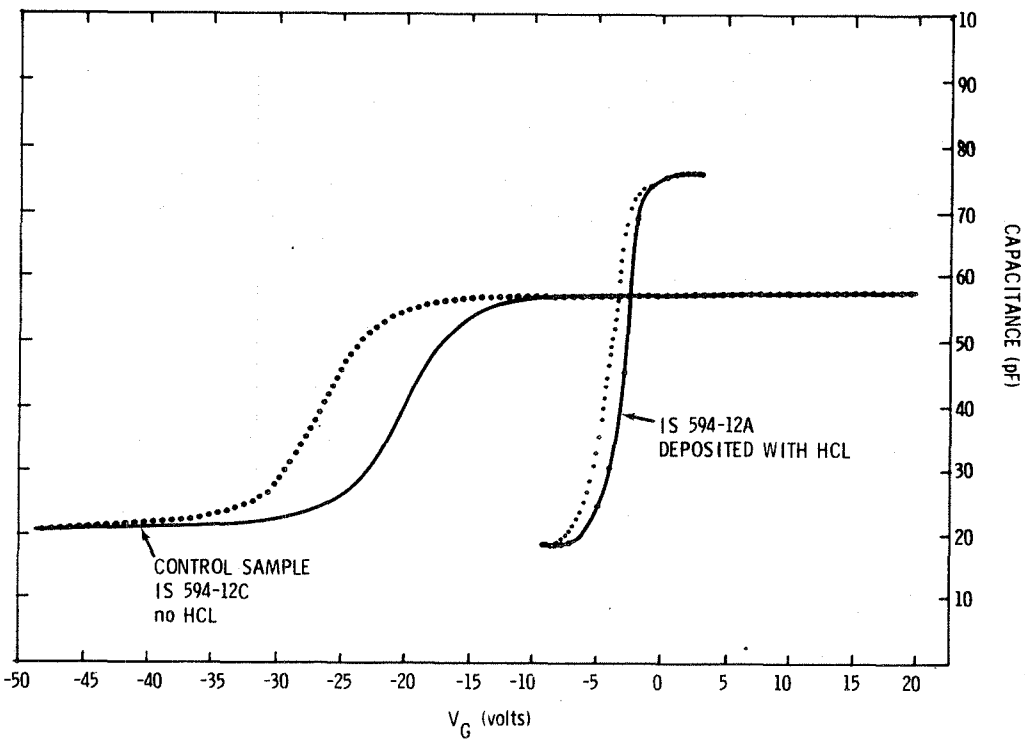

Figure 30. High-Frequency C-V Curves for NOSC Experiment Using HCl in a PECVD Deposition

In order to continue these experiments locally, the Applied Materials AMS-2600 horizontal-flow CVD reactor was modified to handle HCl. Two preliminary depositions were made using standard SiH_4, O_2 and N_2O flow rates of 32 SCCM, 60 SCCM and 22 SLM, respectively. In the first deposition, 13 SCCM of HCl was allowed to flow diluted in N_2 for 300 seconds prior to deposition, and then continued for 60 seconds after the SiH_4 and O_2 were admitted. This resulted in a surface which appeared severely pitted, presumably etched by the HCl. For the second deposition, the same sequence was followed; however, the HCl was

reduced to an unmeasurable trickle of gas. In this case the results were similar. Dilute HCl (5% in nitrogen) was then ordered and new investigations performed.

In the second series of tests, the diluted HCl gas was admitted for periods of 60 to 300 seconds prior to admitting SiH_4 and O_2. The flow was regulated at ~50% of full scale for the same rotometer previously used (actual flow rate is not known). Next, SiH_4 and O_2 were added for 60 seconds and then the HCl gas shut off. The SiH_4 and O_2 were then allowed to flow for a period to achieve an oxide ~1500Å thick, after which capacitors were delineated.

The C-V analysis of these devices was nonconclusive as the devices fabricated with HCl were nearly identical to control devices fabricated without HCl. The result has two possible reasons:

1. the flow rate of dilute HCl gas was insufficient to perform any device improvement, or
2. the oxide fabricated with the HCVD system is already better than the HCl gas can help to obtain.

Considerably more evaluation would be required to prove either of these hypotheses.

Section 4
SBRC HCVD REACTOR MIS EVALUATION

An AMS-2600 horizontal-flow CVD reactor, identical to one at the University of California at Santa Barbara used in earlier years on this and other InSb programs, was installed in SBRC's laboratory. The advantage of this reactor lies in its ability to routinely produce MIS samples with excellent C-V characteristics, with low N_{SS} (on the order of 10^{11} cm^{-2}-eV^{-1}) when the InSb surface has been prepared properly. The films, however, are granular due to the homogeneous nucleation mechanism, which limits the charge transfer efficiency in the InSb imagers. With the reactor now in-house we are able to investigate the dependence of granularity on various deposition parameters such as wafer position, flow rates, and temperature. The reactor provides a control deposition process to monitor the consistency of wafer etching, cleaning, and thin native oxide formation processes. Also, it is to SBRC's advantage to control the maintenance of the CVD reactor.

A preliminary deposition was performed with the purpose of reproducing the MIS C-V characteristics of the UCSB AMS-2600 reactor. Figure 31 is an example of the typical low-frequency and high-frequency C-V curves obtained. The positive flatband shift and the knee in inversion are sometimes observed, but were absent in the initial 77K high-background probe data. A plot of the N_{SS} versus surface potential is shown in Figure 32. This shows a minimum N_{SS} value of 6.5 $\times$ 10^{11} cm^{-2}-eV^{-1}, which is somewhat higher than is normally achieved with the USCB AMS-2600 reactor. Still, for the initial test depositions, the C-V data are considered to be fairly good.

As is normal for the UCSB reactor, the inherent problem with this reactor is the 1000Å diameter granular oxide shown in the SEM photograph of Figure 33.

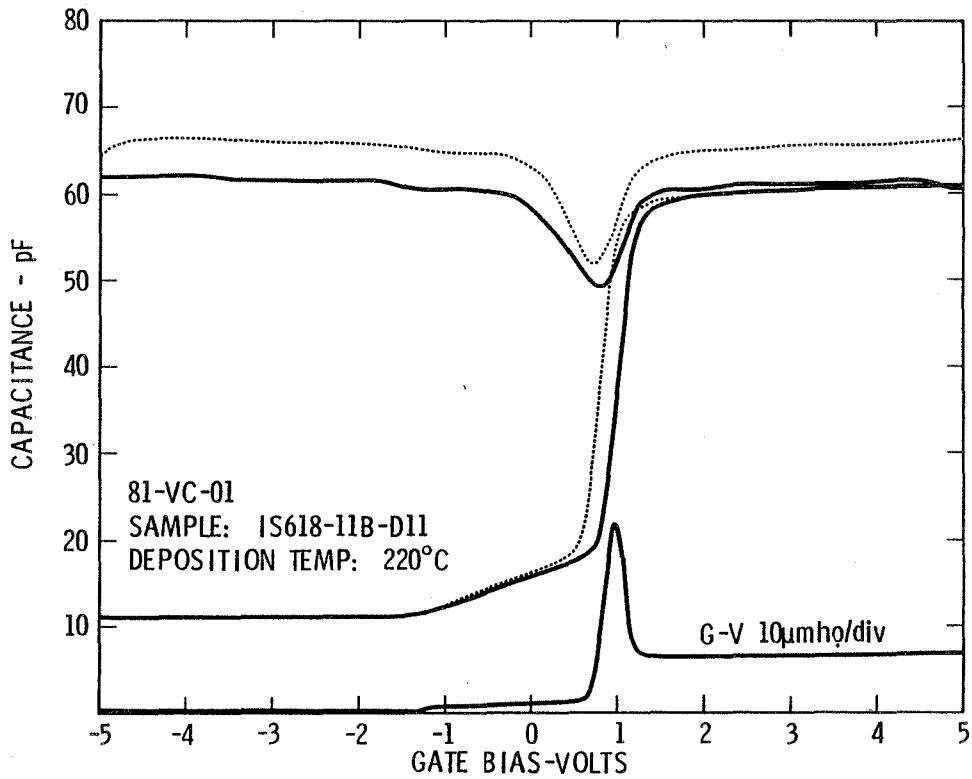

Figure 31. C-V Characteristics of SBRC AMS-2600 HCVD SiO_2 on InSb

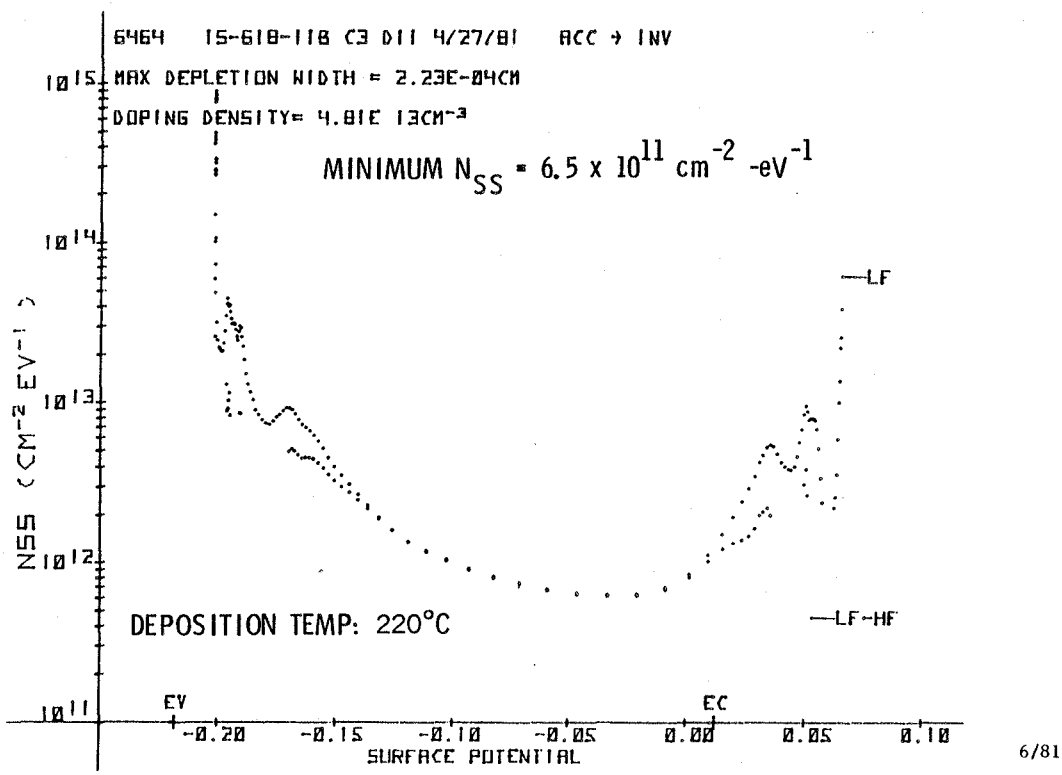

Figure 32. Surface State Density of SBRC AMS-2600 HCVD SiO_2 on InSb

81-6-241

81-VC-01

Sample: IS618-11B

Deposition Temperature: 220°C

Thickness: 1500Å

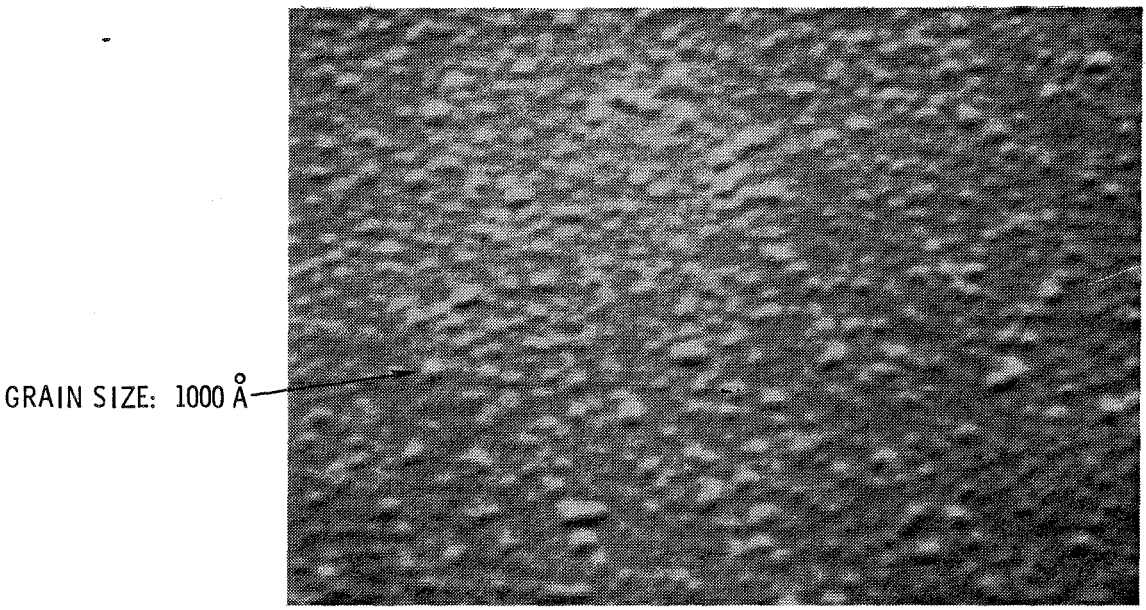

Figure 33. HCVD SiO_2 Granularity from SBRC AMS-2600 Reactor

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Section 5
SBRC SiO_2 INVESTIGATIONS

During 1980, several CVD SiO_2 depositions were performed on a SBRC IR&D program at the Hughes Aircraft facility in Culver City, California. These depositions utilized an alternative CVD method to those used previously on this program. The results of these depositions showed promise of offering an insulator with qualities suitable for ultimately achieving a CTE of 0.999. The films were featureless when inspected with a SEM, and most notably the electrical results were uniform from capacitor to capacitor and run to run. The lowest N_{SS} value achieved was 1×10^{12} cm^{-2}-eV^{-1}, but the deposition parameters were not optimized for InSb, and it was hypothesized this value could be significantly improved with further investigation.

INITIAL SBRC TEMPERATURE-FLOW RATE EVALUATION

During April 1981 a similar system became operational at SBRC. As a first experiment, a matrix investigating various temperatures and flow rates was initiated in order to determine the dependence on these parameters and to find a range in which to concentrate. Initially, temperatures were chosen between 200°C and 250°C. However, due to mechanical limitations of the reactor, these were later changed to range from 150°C to 200°C.

Based on high-frequency C-V results, there is clearly a dependence on temperature and, at a given temperature, on N_2O/SiH_4 ratio. Figures 34 and 35 show C-V curves resulting from depositions at 150°C and 200°C, respectively, with the flow conditions in each case held constant. When the total flow rate is increased, the C-V curves are degraded; however, when the flow rates are changed keeping the N_2O/SiH_4 ratio constant, the C-V curves remain unchanged. As observed in Figures 34 and 35, the lower deposition temperature resulted in reduced hysteresis and V_{FB}.

The improved C-V characteristics also resulted in a decrease in the midband N_{SS} to ~8×10^{11} cm^2-eV^{-1} as shown in the curve of Figure 36. The room temperature leakage of the oxide was measured as shown in Figure 37. From this test, the oxide was found to have a resistivity (ρ) of 1.9×10^{14} ohm-cm.

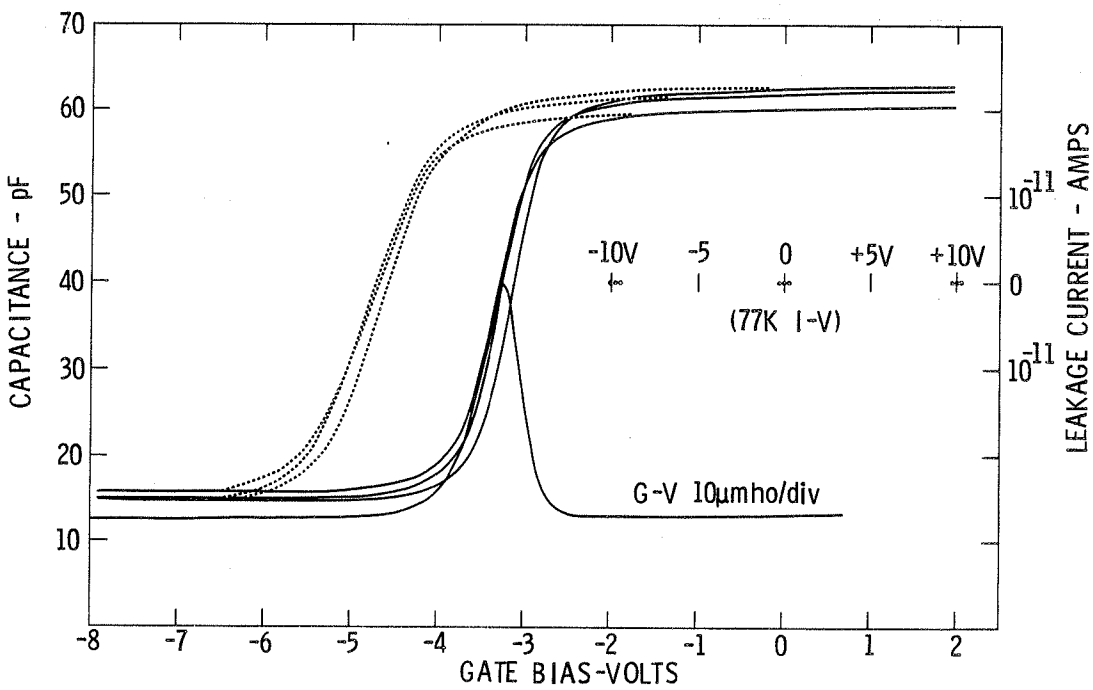


Figure 34. C-V Characteristics of SiO_2 on InSb for a Deposition Temperature of 200°C

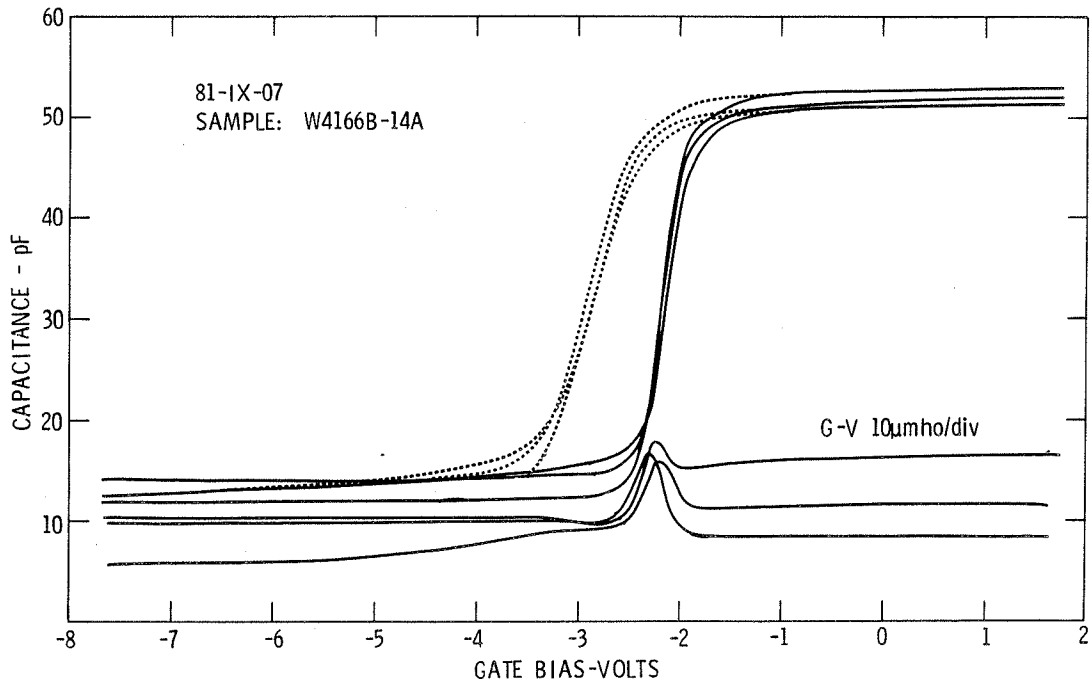


Figure 35. C-V Characteristics of SiO_2 on InSb for a Deposition Temperature of 150°C

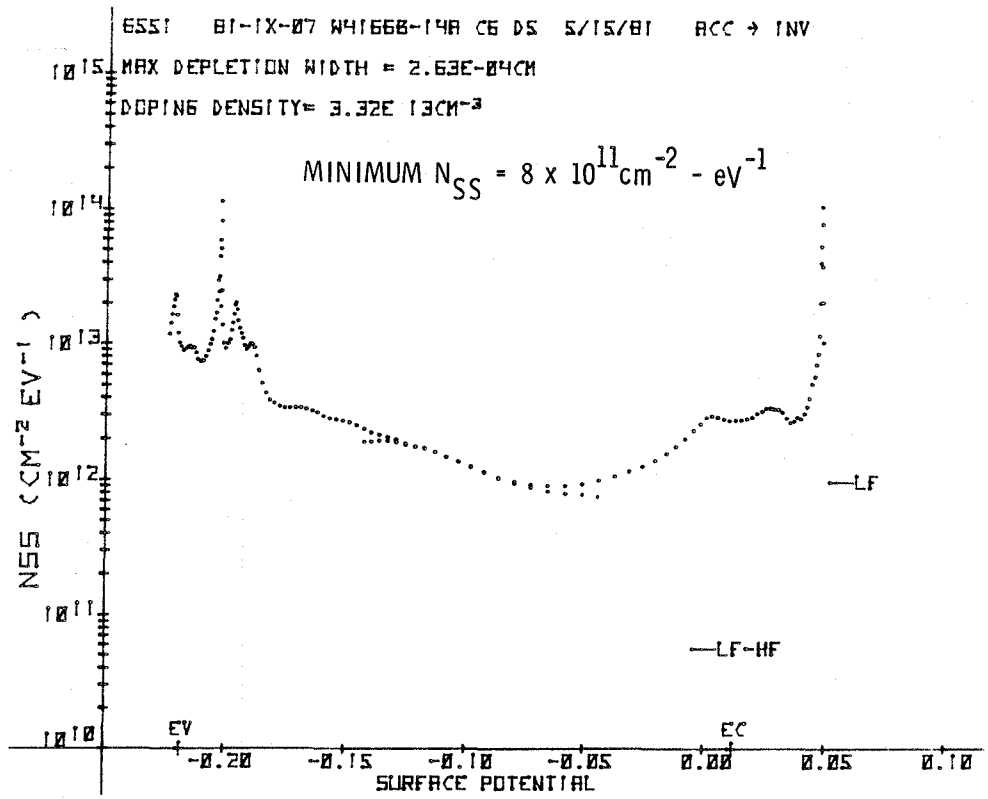


Figure 36. Surface State Density of SiO_2 on InSb as Deposited at 150°C

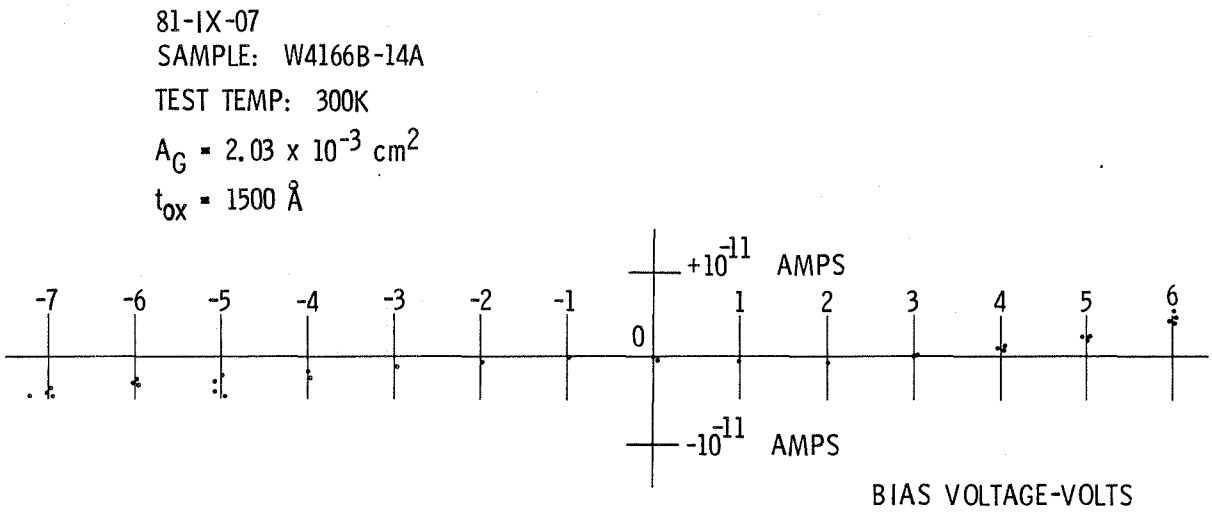


Figure 37. I-V Leakage Characteristic of SiO_2 on InSb as Deposited at 150°C

ANNEALING EVALUATION

A second study in which the effects of subjecting the wafers to a post-SiO_2 deposition anneal process (as discussed by Langan[19]) was performed. Figures 38(a) and 38(b), respectively, show the resulting C-V characteristics for capacitors formed on SiO_2 samples which were unannealed and annealed prior to deposition of the aluminum capacitors; excluding the sputtered SiO_2 layer shown in Figure 5. As is readily seen, the annealed sample has a flatband which was shifted from ~(-)1.8 volts to ~(+)0.8 volt. This corresponds to a change in the fixed charge density (Q_{FC}) from (+)3.05 x 10^{11} charges-cm^{-2} to (-)1.36 x 10^{11} charges-cm^{-2}. In addition, the hysteresis decreased from a delta of ~0.7 volt to <0.2 volt.

An area of concern is observed in the oxide conductance (G-V) peaks. The annealed sample peak is ~9x greater than the unannealed sample. This characteristic proved to be reproducible and is not understood at this time. More sample tests are required to determine the overall effect of this anomaly.

Finally, although attempts were made to perform quasi-static measurements, none were obtained which could be used for determining the surface state density.

SiO_2 GRANULARITY

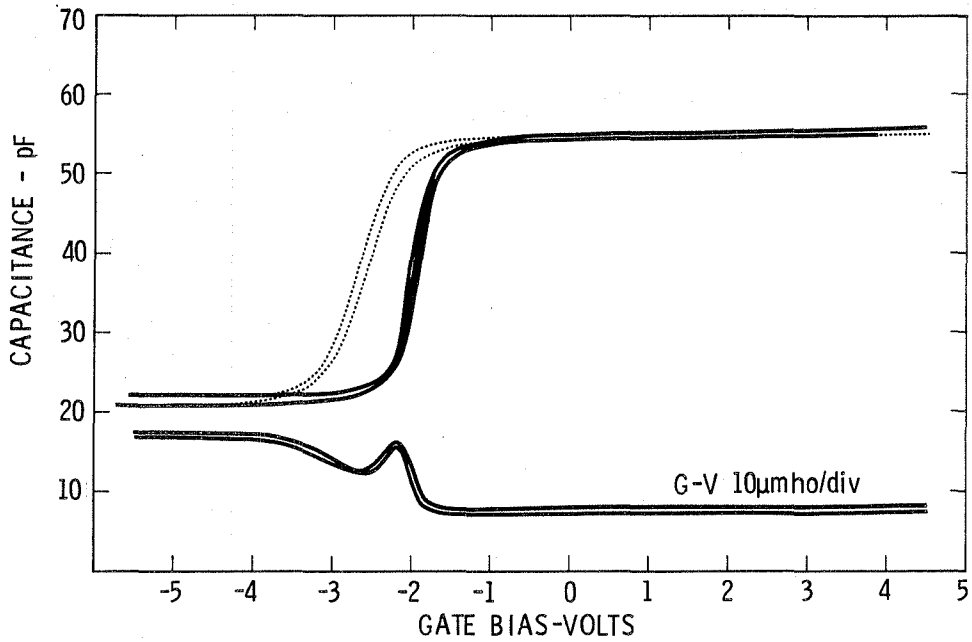
This method of SiO_2 deposition does fulfill the requirement of smooth, nongranular films. Figure 39 shows a scanning electron micrograph of a 1500Å thick SiO_2 film deposited on InSb at 150°C. At the magnification shown, very little structure is discernible. The two visible grains were located for the purpose of focusing and are not typical of the entire surface.

STORAGE TIME EVALUATION

The final item considered was the ability to obtain measurable storage time (T_S) on MIS samples using this insulator. Figure 40 shows a typical capacitance-time (C-t) transient obtained from testing these devices. It shows a 90% T_S of ~11 msec. This value is typical of bulk InSb samples with CVD SiO_2 when tested at 77K. Notably, the storage time was uniform and reproducible from capacitor to capacitor.

81-IX-11
SAMPLE: W4186D-5A

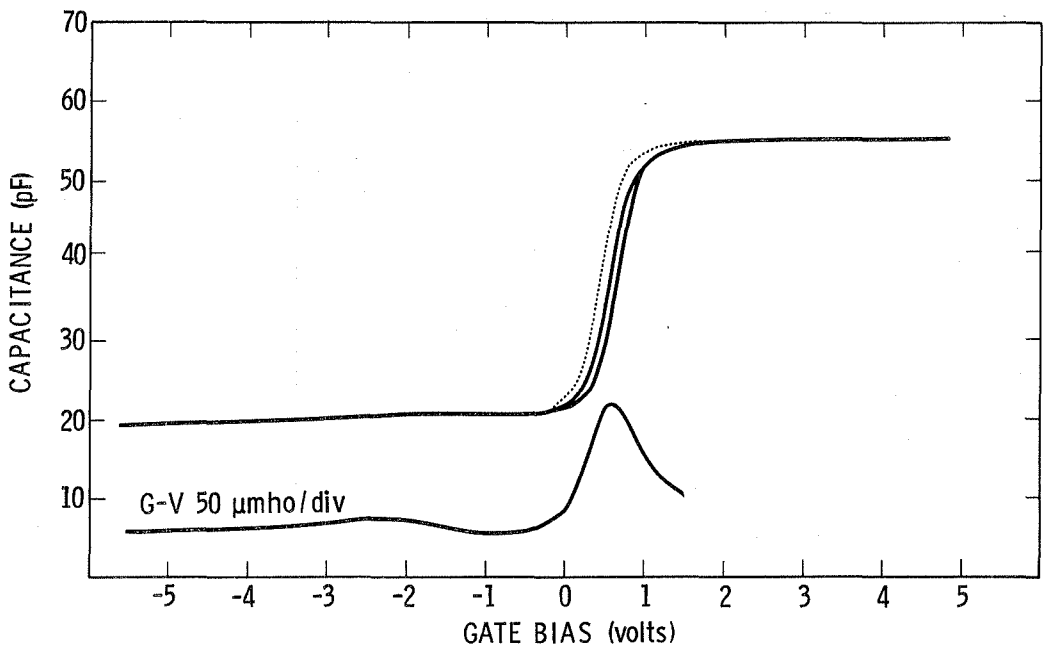
DEPOSITION TEMP: 150°C



(a) Unannealed

81-IX-11
SAMPLE: W4186D-5B

DEPOSITION TEMP: 150°C



(b) Annealed

Figure 38. C-V Characteristics for an Unannealed and an Annealed SiO_2 MIS Sample on InSb

81-IX-07
SAMPLE: W4166B-14B
DEPOSITION TEMPERATURE: 150°C

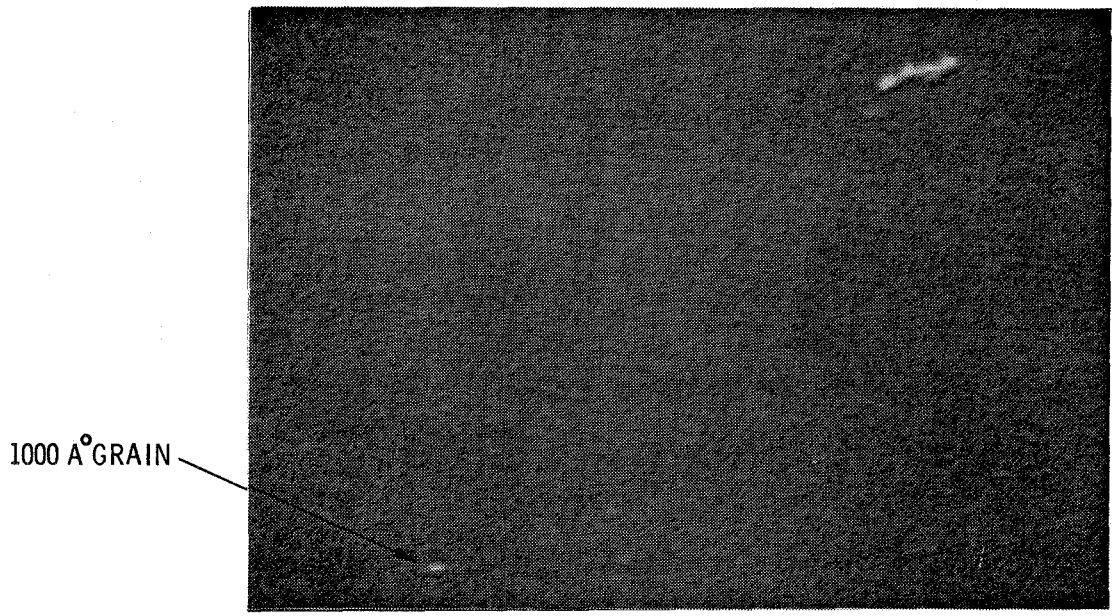
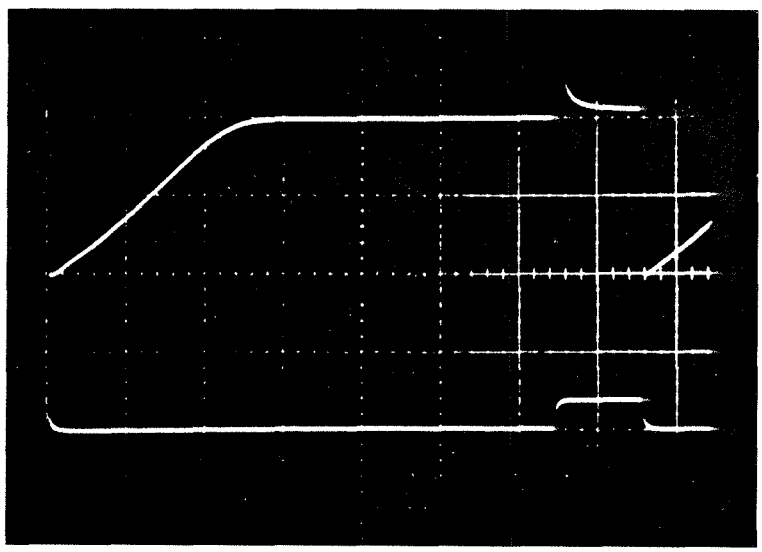


Figure 39. Scanning Electron Micrograph of SiO_2 Granularity

81-IX-07
SAMPLE: W4166B-14A



VERTICAL SCALE
0.5v/div

HORIZONTAL SCALE
5ms/div

RANGE: 50 pF

BIAS: -8 to -10v

81-6-240

Figure 40. Capacitance-Time Transient of an Unannealed SiO_2 MIS Sample on InSb

CONCLUSIONS OF SiO_2 EVALUATIONS

The results of the investigations, using the SBRC deposited SiO_2, show continued promise of ultimately producing an insulator with interface electrical characteristics capable of yielding charge transfer devices with CTE values ≥ 0.999. Although some success was realized by annealing the insulator, as yet the electrical characteristics are not of sufficient quality for use in CCD fabrication. Considerably more investigative work will be required to develop a process which can routinely produce insulators with N_{SS} values in the required range ($\leq 10^{11}$ cm^{-2}-eV^{-1}).

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Section 6
SUMMARY

This report has discussed the efforts pursued in attempting to develop advanced indium antimonide (InSb) monolithic charge-coupled infrared imaging arrays.

The objective of the first task of this program effort was to fabricate a gate oxide with the electrical and physical properties necessary to achieve a charge transfer efficiency (CTE) of 0.999 or greater with InSb IRCCD imagers; that is, to achieve improved performance compared to InSb imagers previously fabricated and delivered to NASA LRC (which displayed a CTE ~0.995). The basic technical approach was to utilize a plasma enhanced chemical vapor deposition (PECVD) process to deposit the gate oxide. This approach was supplemented later in the effort by investigations of (1) horizontal CVD (HCVD) with the addition of HCl gas, (2) an in-house HCVD AMS-2600 system process, and (3) a third SBRC SiO_2 process.

The PECVD SiO_2 process was pursued as the basic approach in order to reduce or eliminate the physical granularity of the gate oxide films, which had been correlated with the lower-than-desired CTEs of the earlier-developed imaging devices. As to this goal, the PECVD process was very successful; operational parameters were established for deposition of smooth, essentially-featureless SiO_2 films when examined by scanning electron microscopy (SEM). Encouragingly, samples with excellent MIS characteristics were also produced early-on in the PECVD investigation, displaying, in fact, better electrical properties than ever before reported for InSb. Unfortunately, although many extensive experiments were carried out with the best control possible over the deposition and system variables, the PECVD SiO_2 gate oxide was found to be nonreproducible from run to run, as well as nonuniform over the InSb wafer surface in a given deposition. Reactant gas premixing was displaying some progress toward the end of the effort in improving the spatial uniformity; however, electrical characteristics and other gate oxide quality measures remained unpredictable over wide limits from one deposition to the next.

In summary, at the conclusion of the gate oxide development effort, the PECVD process was incapable of reliably producing the electrical properties necessary to achieve a CTE of 0.999 when utilized for InSb imager fabrication.

It was concluded that rectifying this situation would necessitate rather major redesign of the LFE PECVD system, modifying the gas dispersion components, introducing platen rotation, and making other changes. The alternative method (3) mentioned earlier was in fact found to show more promise, producing non-granular and highly uniform SiO_2 gate oxides; however, the electrical characteristics achieved by the end of the effort were as yet inadequate for achieving a CTE of 0.999.

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Final Report

16. Abstract

This report discusses the continued process development of SiO_2 insulators for use in advanced InSb monolithic charge-coupled infrared imaging arrays. Specific investigations into the use of plasma enhanced chemical vapor deposited (PECVD) SiO_2 as a gate insulator for InSb CCDs is discussed, as are investigations of other CVD SiO_2 materials.

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19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unlimited	66	

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